KU LEUVEN BRUGGE

m·group

EXTENDING A PROCESSOR FOR RELIABLE EMBEDDED SYSTEMS

1 ASSIGNATION

Number of students: 1
Type of project: Master's thesis

2 DESCRIPTION

Embedded systems are commonly used in both general-purpose and safety-critical applications. Due to technological advances, these embedded devices utilize extremely small components and operate on low voltages. This, however, makes them more susceptible to external disturbances such as electromagnetic interference, temperature fluctuations and the impact of high-energy ionizing particles. These disturbances can result in single-event upsets, such as a bit flipping inside a CPU register, which can in turn lead to corrupted data or control flow, and unexpected and unpredictable system behavior.

The M-Group research group at KU Leuven Bruges has extensive experience in making embedded systems more resilient to these types of upsets by implementing error detection techniques within the embedded software executing on the system. These techniques insert extra instructions into the software that allow for verification of the program's data and control flow.

A downside of these techniques is that their implementation is limited by the instructions available in the target instruction set architecture (ISA), making techniques with more complex mechanisms infeasible to use in reality. Moreover, to implement the techniques, registers must be made unavailable to the compiler, sometimes limiting the programs that can be compiled and hence executed on the embedded system.

In recent years, extensible or customizable processors/ISAs have emerged, like RISC-V and Cadence Tensilica. With such customization, the implementation of the aforementioned error detection techniques can be enhanced. The M-Group group is currently investigating ways to extend the RISC-V ISA with specialized instructions to support various error detection techniques.

The DistriNet research group of KU Leuven developed a highly extensible FPGA-friendly RISC-V processor model called Proteus that allows for easy experimentation with hardware extensions. The core implements the RV32IM instruction set as a classic 5-stage RISC pipeline (Fetch, Decode, Execute, WriteBack). This is all implemented in the SpinalHDL hardware description language.

The goal of this project is to extend the Proteus processor with specialized instructions to support various error detection techniques. The implementation should be optimized to impose as little overhead as possible.

To verify the implementation, a test bench should be written to test if all instructions work as expected. Next, several programs utilizing the custom instructions should be tested on the synthesized FPGA to verify that they result in a correct output.

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Research group: M-group (iiw.kuleuven.be/onderzoek/m-group)

3 EXPLORATION

The Proteus processor model is available on GitHub.
Documentation on SpinalHDL is available via: [link].
More info on the upset resilience track can be found in papers authored by Brent De Blaere, Mohaddaseh Nikseresht and Jens Vankeirsbilck: [link].

4 FOCUS

Processor design, Resilience, soft error detection, vulnerability analysis

5 GOAL

At the end of this project:

- The student should have researched which instructions can be defined to aid with the detection of upsets
- The Proteus processor model should be synthesized on an FPGA.
- The Proteus processor model should be extended with support for the custom instructions and synthesized on an FPGA
- The correct operation of the implementation should be verified

6 ORGANIZATION

The project will be organized at the M-Group research group.