IEEE Windsor Section

Research Centre for Integrated Microsystems
University of Windsor

Dr. Andreas Kugel

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Date & Time: May 15th 2015, 10:00 AM – 11:00 AM
Venue: **CEI 2100**.

Academic Biography:

Since 2009: Academic staff memeber, Heidelberg University. Head of the FPGA group of the Dept for Computer Science V, Prof. Dr. Männer. Research group spokesperson. 1991 through 2009: Technical staff member, Mannheim University. Since 1997 head of the FPGA group of the Dept for Computer Science V, Prof. Dr. Männer 1985 through 1990: Hardware/software design engineer, COMSOFT GmbH, Karlsruhe.

Previous Projects:

Design, implementation, production and programming of the data-acquisition module "ROBIN" of the ATLAS experiment at the LHC, CERN.

Design of the data-acquisition architecture of the DSSC detector at DESY, Hamburg.

Designing, implementation and production of the FPGA coprocessors MPRACE1 and MPRACE2.

Conceptual work on the hybrid architecture "GRACE" targeted at astrophysical simulations.

Design, implementation and prototyping of the FPGA coprocessor system ATLANTIS targeted at fast track-recognition at the ATLAS experiment at the LHC, CERN.

Title:

Evaluation of Xilinx Vivado high-level-synthesis to design a TCP/IP protocol engine.

Abstract:

High-level-synthesis (HLS) tools are essential to enable profiting from FPGA-technology in mainstream computing applications. To date, problems with regular patterns of data access and computation can be handled, at least to a certain extent, using state-of-the-art tools like OpenCL, Vivado HLS and others. Reliable, high bandwidth, low latency data transmission is a common issue in many Physics experiment and many actual solutions involve FPGA technology.

However, the requirement on reliability is frequently sacrificed in favor of bandwidth and low latency, due to the complexity of the issue. and custom or simple standard networking protocols like UDP are employed. This work tries to assess the applicability of Vivado HLS to implement the reliable TCP/IP networking protocol starting from a software model in "C". Major topics to be addressed are implementation of the TCP state machine and buffer management. Results of a TCP data transmitter prototype implementation on a Xilinx Zynq evaluation board shall be presented.