Title of invited talk	**Prospects of Carbon Nanotube Field Effect Transistor (CNFET)**
Abstract	CMOS technology scaling driven by the benefit of integration density, higher speed of operation and lower power dissipation, has passed over many barriers over the past four decades. Presently, it is facing even more obstacles, which are more acute than earlier ones. Few of them are variability, subthreshold leakage, gate-dielectric leakage, SCE (short-channel effect) or DIBL (drain-induced barrier lowering). The variability is becoming a metric of equal importance as power, speed, and area. To overcome these issues, researchers are exploring new devices and structures for replacing the classical CMOS technology. CNFET (Carbon Nanotube Field Effect Transistor)are the promising technologies of choice to replace classical CMOS at the nanoscale level. The primary advantage of CNFET is the high mobility of charge carriers and the potential to minimize the subthreshold slope (i.e., minimize the short channel effects). Initially, lot of fabrication issues was existing in CNFET technology. However, most of the fabrication issues like positioning and alignment of CNTs along with the presence of metallic CNTs have been solved.Moreover, CNFET can be fabricated using the existing Si-CMOS infrastructure and it can also be integrated with Si-CMOS on the same chip. It means that most of the fabrication issues have been solved and CNFET technology holds a lot of promise.