**CMOS Technology Scaling and Power Management Issue**

There has been a tremendous growth of semiconductor industry following the invention of bipolar junction transistor in 1947 and integrated circuit in 1958. VLSI era started with nMOS technology in the 1970s; most of the early processors were built using nMOS technology. The first microprocessor to use CMOS was RCA 1802 COSMAC, an 8-bit processor; but first powerful 32-bit microprocessor built in CMOS technology was Bellmac-32 in 1982. Before about 1985, CMOS was considered to be expensive and slow technology and was used only in applications requiring either very low power or radiation hardening. Since then, CMOS technology dominated the market particularly for logic circuits and semiconductor memories. Scalability of CMOS technology resulted in not only miniaturization of the integrated circuits making them affordable but also high functionality and performance of such circuits.

In this lecture, a brief introduction of the principle of CMOS technology scaling will be made. This will be followed by a discussion of the traditional solutions, e.g., gate oxide scaling, increase in channel doing, reducing junction depth etc., used to overcome different issues faced by the technology in the early years of scaling. The traditional solutions started becoming ineffective in the latter half of the first decade of the new millennium when alternative scaling involving innovations in materials and devices structures e.g., strain technology, high-k gate dielectric & metal gate, 3D device structure (FinFET) etc., were introduced. At present, power management has become the major concern for further scaling of the technology. The origin of such concern along with the possible solutions will be discussed.