Title: Compact/SPICE Modeling from a FOSS TCAD/EDA perspective

Abstract: Compact/SPICE models of circuit elements (passive, active, MEMS, RF) are essential to enable advanced IC design using nanoscaled semiconductor technologies. Additionally, compact/SPICE models are used to facilitate communication between the semiconductor companies and fabless IC design teams. To explore all related interactions, we are discussing selected FOSS CAD tools along complete technology/design tool chain from nanascaled technology processes; thru the semiconductor devices compact modeling; to the advanced analog/RF IC transistor level design support. New technology and device development will be illustrated by application examples of the FOSS TCAD 3D numerical simulators Compact modeling will be highlighted by review topics related to its parameter extraction and standardization of the experimental and measurement data exchange formats. Discussing new model implementation into the FOSS EDA simulators, we will also address an open question of the compact/SPICE model Verilog-A standardization. Next, we will also show the FOSS CAD tools for designing and simulating analog/RF ICs. Application and use of these tools for advanced IC design, including analog/RF IC applications, directly depends on the quality of the compact models implementations in these tools as well as reliability of extracted models and generated libraries/PDKs. We will highlight upcoming opportunities and benefit using open-source hardware, ASICs and ICs design using open-source 130nm CMOS process libraries/PDKs. This presentation is intended to be of direct use to the engineers and researchers involved in the development of compact/SPICE models as well as integrated circuit designers in particular at the transistor level. As a result of the talk, we expect further discussion on the compact/SPICE Verilog-A standardization to encourage cross-regional development of the FOSS TCAD/EDA tools.