Book of Proceedings

4th International Conference

on

2021 Devices for Integrated Circuit (DevIC 2021)

Organized by

IEEE KGEC Student Branch Chapter in association with

Department of ECE, KGEC

19-20th May, 2021

Kalyani Govt. Engg. College

Contents

DevIC 2021 Registered Paper's List:

About Kalyani Government Engineering College

Kalyani Government Engineering College was established by Govt. of West Bengal in the year 1995. KGEC is an autonomous institute affiliated to Maulana Abul Kalam University of Technology (MAKAUT) formally West Bengal University of Technology (WBUT). KGEC is among the top engineering colleges of West Bengal. It is one of the finest engineering institutes in the country, it is a community of learners, striving to educate the mind, nurture the spirit, and foster the development of whole individual.

KGEC has 10 academic departments, offering B.Tech, M.Tech and MCA programs. KGEC has about 1700 students, 120 teachers, 100 technical and supporting staff members. We have more than 50 labs and 10 research facilities in the college.

Conferences, workshops, seminars and academic fairs are held on a regular basis in the campus. KGEC is known for producing industry ready professionals every year. And, the institute has an excellent placement record in the past several years.

Kalyani Government Engineering College has a beautiful lush green pollution free campus spawning over 75 acres, which is located on the northern periphery of University of Kalyani. KGEC is a non-residential institute that has six hostels (five for boys and one for girls) equipped with all modern facilities such as gyms, libraries, television sets, computer rooms, high speed internet connectivity, indoor and outdoor sports, etc.

KGEC has state of the art well maintained infrastructure with all the modern facilities for the students like smart classrooms, interactive conference rooms etc. Library and laboratories are connected to LAN.

KGEC is one of the finest engineering institutes in the country. It is a community of learners, striving to educate the mind, nurture the spirit, and foster the development of whole individual. We has a distinctive atmosphere where the emphasis is on teamwork, cooperation, and friendly competition. Smaller student groups in classes and laboratories helps students develop close supportive relationship with each other as well as the faculty members.

The campus life of KGEC is perfect mix of relaxation, extra-curricular activities along with rigorous academic activities. Here, at KGEC students focus not only on the curriculum but also on extracurricular activities like sports, NCC(National Cadet Corps), NSS (National Service Scheme) etc apart from studies.

IEEE Kalyani Government Engineering College Student Branch Chapter

About IEEE: The IEEE is the world's largest technical professional society, connecting more than 400,000 members to the latest information and the best technical resources available. From continuing education courses and certifications, to conferences and competitions, one can learn more, create more, and achieve more of what matters in your life and career through IEEE membership. IEEE membership helps support the IEEE mission of promoting the engineering profession for the benefit of humanity and the profession.

IEEE Student Branch Chapter: An IEEE Student Branch provides opportunities to meet and learn from fellow IEEE Student and Graduate Student Members and engage with professional IEEE members locally. An active IEEE Student Branch can be one of the most positive elements of your academic career, offering programs, activities, and professional networking opportunities that build critical skills outside of the classroom. IEEE currently has Student Branches at thousands of universities and colleges in hundreds of countries throughout the world.

Benefits of forming an IEEE Student Branch Chapter: An IEEE Student Branch gives students a community of peers, and a connection to faculty and industry professionals who drive innovation in countless technical fields. Student involvement in Branch activities, whether special projects, social and technical meetings, outreach programs, conferences, local Section or Regional opportunities, etc. can help develop a record of accomplishment and capabilities beyond the norm.

Goals of IEEE KGEC Student Branch Chapter

- Opportunities to network on a local level
- Obtain funding for events, projects, and activities
- Develop projects and obtain sponsorship based on your IEEE affiliation
- Receive support for hosting professional awareness programs
- Connect with other likeminded student groups to advance the IEEE mission

In addition, IEEE KGEC SB Chapters offers programs and projects that keep students interested in the Branch and its activities and their chosen profession.

Since its inauguration on November 14, 2014, IEEE Student Branch chapter of Kalyani Government Engineering College has organized several International Conferences, Mini-Colloquium (MQ), Distinguished Lecture talks, Workshop, seminars and Industry-Academia Innovative practice Lecture-talk program for the benefit of the students.

Vice Chancellor's Message

It is indeed a pleasure to greet you all during the 4th International Conference on ''2021 Devices for Integrated Circuits (DevIC 2021)'' on 19-20 May, 2021 at Kalyani Government Engineering College, Kalyani. At the outset, I would like to express my sincere gratitude to the distinguished members of the organising committee who have gone to extreme lengths to make this conference a grand success.

The conference is of immense help to the researchers and students to enrich their knowledge domain and broaden their horizon.

I would like to take this opportunity to congratulate the entire team for their commendable work in organisation of this conference and wish the conference all the success.

Date: May 6 th, 2021

Kalyani- 741249

Professor Saikat Maitra

Vice Chancellor

Maulana Abul Kalam Azad University of Technology

Message from the Principal, Kalyani Government Engineering College

I am extremely happy to note that IEEE KGEC Student Branch Chapter in association with Department of Electronics & Communication Engineering of Kalyani Government Engineering College is organizing 4th International Conference "**2021 Devices for Integrated Circuit (DevIC 2021)" on 19-20th May, 2021.**

I am extremely confident that DevIC 2021 will be a major conference organized to bring together researchers, developers and practitioners from academia and industry working in the area of electron devices and circuits.

I congratulate all associated with the DevIC 2021 for their untiring efforts in organizing this Conference and wish the Conference all success.

Dr. Sourabh Kumar Das
Principal, Kalyani Government Engineering College
Chief patron, DevIC 2021

Message from General Chair, DevIC 2021

On behalf of the entire organizing committee, I would like to take this opportunity to welcome you to the 4th **International Conference on "2021 Devices for Integrated Circuit (DevIC 2021)"**to be held on 19-20th May, 2021 in Kalyani Government Engineering College. Serving as the General Chair of DevIC 2021 I feel the immense importance of opportunities like these that serve as an auspicious moment for budding researchers to come up with fresh and revolutionary ideas to address current concerns. The young researchers would highly benefit from the fathomless knowledge of the experts and for the sagacious delegates this serves as an opportunity to witness the unfettered imagination of fledgling researchers. We are grateful to the technical program committee members and other reviewers who put forward their efforts in recruiting papers, reviewing submissions, and made valuable remarks that helped in enriching the quality of the conference. I would like to appreciate the persistent support from the organizing committee and inconspicuous contributions from several other members who have conjointly made this conference a grand success.

Finally, I extend my sincere gratitude to all the keynote speakers and luminaries who have spared their invaluable time to attend this conference. I hope your presence will serve as an inspiration to the nascent minds of the scientific community and make this conference a grand success.

Entwined with the lingering charm of Kalyani, I hope this conference serves to be an enriching and delightful experience.

Dr. Angsuman Sarkar
General Chair, DevIC 2021
Branch Counselor, IEEE EDS KGEC SB Chapter

Message from the Head of the Department of Electronics & Communication Engineering

The continuous development of semiconductor technology and applications has significant impact on daily life in the twenty first century. Fifth-generation (5G) wireless cellular technology, hardware-based Artificial Intelligence, advanced devices for Internet of Things (IoT), nanoscale devices, sensors and networks are some of the recent developments those necessitate high performance integrated circuits . Design and application of high performance integrated circuits require expertise in a number of different areas which include devices made of new materials, non-CMOS devices & technologies and heterogeneous integration. Present international conference on Devices for Integrated Circuit (DevIC), 2021, organized by IEEE KGEC Student Branch Chapter in association with the Department of Electronics & Communication Engineering , Kalyani Government Engineering College and technically co-sponsored by IEEE EDS Kolkata Chapter is aimed to bring together academicians , technologists and researchers of different aspects of semiconductor devices and integrated circuits, on a common platform to share their knowledge for future progress in this research area of extreme significance. It is a challenging task to conduct international conferences like the present one in this global pandemic situation due to Covid19. However, we hope this virtual conference is going to be a great success like the previous three DevIC conferences. I extend my sincere regard and thankfulness to each dignitary and participant and wish every success of this international conference.

Prof. (Dr.)Sukla Basu

Head, Electronics & Communication Engineering Department

Kalyani Government Engineering College

Key Factors of the DevIC 2021:

❖ **DevIC 2021** brings together researchers, educators, students from across academia, government, industry and non-governmental organizations to discuss share and promote current works and recent accomplishments across all aspects of the **Electron Devices and circuits**.

❖ **Low Registration Fee** (IEEE Member=Rs 2800/- only; Non-IEEE member= Rs 3500/-; Student Member= Rs 2100/-)

❖ **High Percentage of Rejection: 49%**

❖ Assigned Total **143 Reviewers** from India and Abroad. Approx. 25% of total Reviewers are from Abroad and the rest are from India.

❖ Each manuscript has been reviewed twice or thrice. In brief almost 59**% of the total papers have been reviewed thrice**.

❖ Each and every manuscript has been checked for Plagiarism and Similarity Reports have been generated using the **CrossCheck®**.

❖ To enhance the quality of the conference, **6 Plenary Talks** have been scheduled in DevIC 2021.

❖ All the accepted papers will be submitted for inclusion into **IEEE Xplore** after being presented in the conference

❖ Total **Twelve (12) journals** have shown their interests to publish the extended version of selected papers from DevIC 2021. Out of the eleven journals, **Six (6) journals are SCI indexed, One (1) journals are Emerging SCI indexed and Three (3) journals are Scopus Indexed**.

❖ Almost **Twenty Five (25) Honourable IEEE EDS Distinguished Lecturer (DL)** and **Fifteen (15) Honourable IEEE Fellow Members** are associated with DevIC 2021.

List of the Invited Speakers at DevIC 2019

Prof. Paul R. Berger, Ph.D.
IEEE Fellow; IEEE Distinguished Lecturer, IEEE EDS Board of Governors (‘19-‘21), VP Strategic Directions IEEE EDS (’20-’21), Founder, Nanoscale Patterning Laboratory, Director, Nanoelectronics and Optoelectronics Laboratory (NOEL), Director, Organic and Printed Flexible Electronics Laboratory (OPFEL), Department of Electrical and Computer Engineering, Department of Physics, Ohio State University

Dr. Wladek Grabinski (Senior IEEE EDS Member, MOS-AK (EU))
IEEE EDS Distinguished Lecturer

Prof. Alexander Kloes
Head of research group Nanoelectronics / Device Modeling
Technische Hochschule Mittelhessen, Germany, Giessen

Dr. Daniel Tomaszewski (IEEE EDS Newsletter Editor-in-Chief)
Łukasiewicz Research Network – Institute of Microelectronics and Photonics Al. Lotników 32/46, 02-668 Warsaw, Poland Department of Microsystem Technology ul. Gen. Leopolda Okulickiego 5E, 05-500 Piaseczno, Poland

Dr. Maria Serena Chiriacò
CNR NANOTEC Institute of Nanotechnology, via Monteroni, Lecce, 73100, Italy

Prof. Subhankar Paul, Ph.D.
Professor, Department of Biotechnology and Medical Engineering,
Chief Investigator, Structural Biology & Nanomedicine Laboratory,
National Institute of Technology Rourkela, Orissa, India

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DevIC 2019

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- **Dr. Sourabh Kumar Das** (Principal, Kalyani Government Engineering College, Kalyani, India)

Patrons:

- **Dr. Chandan Kumar Sarkar** (Professor, Jadavpur University & Chair IEEE Kolkata Section, Kolkata, India)
- **Dr. Achintya Das** (Professor, Kalyani Govt. Engg. College, Kalyani, India)
- **Dr. Sukla Basu** (Professor & Head of the Department of ECE, Kalyani Govt. Engg. College, Kalyani,India)

Honorary Chair:

- **Mr. Deepak Mathur (**IEEE Region 10 Director-Elect 2019-2020)
- **Dr. Meyya Meyyappan (**President IEEE EDS HQ USA, Chief Scientist, NASA Ames Research Center, Center for Nanotechnology)
- **Dr. MK Radhakrishnan** (Secretary, IEEE Electron Devices Society, IEEE EDS Distinguished Lecturer)

General Chair:

- **Dr. Angsuman Sarkar** (Chair, IEEE EDS Kolkata Chapter, Kolkata, India, SMIEEE, Associate Professor, Kalyani Govt. Engg. College)

General Co-Chair:

- **Dr. Manash Chanda** (Secretary IEEE EDS Kolkata Chapter)
- **Prof. Sandip Nandi** (Dept. of ECE, Kalyani Govt. Engg. College, Kalyani, India)

Program Chair:

- **Dr. J. K. Mandal** (Professor of Computer Science & Engg., former Dean, Faculty of Engineering, Technology and Management, Kalyani University, India)
- **Dr. Debasish De** (Professor, MAKAUT, Kolkata, India)

Convener:

- **Dr. Krishnendu Chakrabarty** (Principal, Govt. College of Engineering and Ceramic Technology, India)
- **Dr. Subir Kumar Sarkar** (Professor, Jadavpur University, Kolkata)

Co-Convener:

- **Dr. Bishnu Pada Biswas** (Registrar, Kalyani Govt. Engg. College, Kalyani, India)

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- **Prof. Benjamin Iniguez** (IEEE Distinguished Lecturer (EDS), University Rovira i Virgili, Spain)
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Hard and Soft Switching Geometries For Operations of the MOSFET Used For the SMPS

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Abstract: The paper re-validates in between hard and soft switching activities, geometries and characteristics generated by the switching actions of the MOSFET used for the boost converter as switched mode power supply (SMPS) reshaped by published literature with huge reviews & study. The parasitic effects, stresses and switching power losses across the power semiconductors are higher than soft switching operations of the SMPS. So, the soft switching boost converter for high switching frequency that needs for the high power density and compact size as performance improvements in a platform.

Keywords*: Hard switching & Soft switching operations, Switching curves of MOSFET, Wide comparisons & SMPS*

Suitability of the Static Converters For the Power Factor Correction (PFC)

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Abstract: In this paper, suitability of the static converter topology along with structures and applications are proposed to assess the power factor (PF). Various issues of the static converters are framed out by gross evaluations on the power factor correction (PFC) and quality improvements. The power quality judgments and indices are co-related by the high power factor to boost the stability and reliability of the power distributions as suitability and objective of the paper

Keywords*: Power factor, Static converters for the PFC, Performance evaluations & Improvements*

Generation of Tunable Low-noise Millimeter-wave Signal using Optical Frequency Comb through Electrical Mixing at 94 GHz

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Abstract: In this paper, millimeter-wave signals are generated with characteristics of high gain and low noise using optical frequency comb, where generated signals are tunable at a wider range (approx 50 Hz in both the sides) around the central frequency 94 GHz. Concept of electrical mixing is incorporated to achieve the tuning of the signals. Result shows that adopted methodology is far superior to conventional optical mixing where stable, high gain and low noise microwave signals are obtained in all the tuned frequencies. Wider tuning range speaks about the supremacy of the proposed scheme both in optical as well as in RF spectrum.

Keywords: *Tunable signal; Millimeter-wave spectra; Lownoise; High gain,; Electrical mixing; Frequency comb*

Swastika Shaped Broadband Dielectric Resonator Antenna for S,C,X & Ku Band

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Abstract: High gain, broadband Swastika Shaped Dielectric Resonator Antenna (SSDRA) using barium zinc tantalate ceramic (εr = 30) is designed and analyzed in this paper. A Small Air gap is introduced in this structure and the effect of the air gap is also investigated here. The operating frequency of this antenna (SSDRA) is 4.3GHz – 18GHz with an impedance bandwidth of 122% at -10dB return loss which covers S- band to Ku Band. The maximum Gain of 9.21dBi is achieved with this Swastika Shaped structure. When a small air gap is introduced at the central position of every edge keeping all dimensions the same, the operating frequency range increases to 3.736GHz-18.575GHz (bandwidth 133%) with a slight reduction in maximum gain (9dBi). A Microstrip line is used to feed the SSDRA. Simulation of all structures is done using CST Microwave Studio Software. Performance parameters of the proposed structure are compared with those of several wideband DRA structures reported in recent literature.

Keywords: Swastika Shaped Dielectric Resonator Antenna 1; *Broadband Antenna 2; High Gain Antenna 3*

Study of 2D Electron Mobility in AlGaN/GaN Quantum well Structure

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Abstract: We study the electron mobility μ of AlGaN/ GaN quantum well (QW) based field effect transistor structure by considering potential profile V(z) taking the effect of polarization (V_{pol}) and also 2D electron density N_s (through Hartree potential) V_{pol+ns}. N_s relates to the Fermi energy E_F which affects μ. The change in V(z) affects the population of subband electron energy level and wave function. Accordingly, the alloy disorder and interface roughness scattering potentials are influenced. We show that $\mu(V_{pol}) > \mu(V_{pol+ns})$. Increase in N_s increases μ. In case of $\mu(V_{pol+ns})$ there is a decreasing trend at larger N_s due to dominance of alloy scattering effect which matches the experimental results.

Keywords: *GaN/AlGaN HEMT structures; Nitride quantum wells; Polar semiconductors; Electron mobility; 2D electron gas density (2DEG).*

Oscillating Electron Mobility in Double V-shaped Quantum Well based Field Effect Transistor Structure

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Abstract: The electron mobility μ exhibits oscillatory behavior with gate electric field F in an asymmetrically doped double V-shaped $Al_xGa_{1-x}As$ quantum well field effect transistor structure. By changing F, single-double-single subband occupancy of the system is obtained. We show that μ oscillates within double subband occupancy as a function of F near resonance of subband states due to the relocation of subband wave functions between the wells through intersubband effects.

Keywords*: Mobility oscillation, V-shaped quantum well, Gate electric field.*

Analytical Investigation Of Trenched Multi-layered Gate Silicon On Nothing MOSFET With Graded Work-function

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Abstract: This paper presents a silicon based grooved multi-layered gate architecture with air as buried oxide layer to improve the self-heating effect (SHE) and also capable of enhancing the short channel effects (SCEs). This structure takes the benefit of the trenched stack gate to decrease the hot carrier effect (HCE) and linearly varied work-function along the gate region to enhance the carrier transport efficiency. An analytical model is formulated for the presented graded work-function (GW) trenched rectangular stacked gate (TRSG) silicon on nothing (SON) MOSFET and validated through TCAD device simulator. The proposed device performances are upgraded with its physical parameters like negative junction depth (NJD). The performance parameters of GW-TRSG SON MOSFET are compared with trenched rectangular gate (TRG) silicon on insulator (SOI) MOSFET in terms of sub-threshold parameters, electron mobility, and higher-order trans-conductance for better linearity and proficiency.

Keywords*: Silicon-on-insulator; Trenched gate; self-heating effect; Short channel effect; Silicon-on-nothing.*

Design and Comparative analysis of a Two-Stage Ultra-Low-Power Subthreshold Operational Amplifier in 180nm, 90nm, and 45nm technology

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Abstract: In this paper, a two-stage ultra-low-power operational amplifier is designed, and a comparative analysis of the proposed subthreshold complementary amplifier is presented between 180nm, 90nm, and 45nm CMOS technology. The proposed operational amplifier is compared across several different parameters to determine the optimal design. It achieves a maximum gain of around 75 dB and a phase margin of 76°, dissipating just 140nW with a supply voltage of 0.5 V which is well suited for biomedical applications that require low power and high gain. The proposed operational amplifier has been designed using a SPICE-based circuit simulator.

Keywords*—Ultra-low power, high gain, low voltage, operational amplifier, subthreshold operation, bio-amplifier, neural sensing*

Impact of Source Side Cavity on Sensitivity of Hetero Channel Double Gate MOSFET Biosensor

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Abstract: In this paper, a dielectric modulated hetero channel (InP/InGaAs/InP) MOSFET with source-side cavity (DM-H-SC) biosensor is presented for identification of biomolecules like uricase, streptavidin, Ferro-cytochrome, and Protein. In the proposed structure, neutral biomolecules are simulated with their respective dielectric constants but charged biomolecules are simulated with both dielectric constant and charge density. Numerous electrical features such as surface potential, electric field, threshold voltage, and sensitivity of the proposed device have been estimated using the 2D TCAD platform. The highest sensitivity of 0.52 is realized for protein in comparison to uricase, streptavidin, Ferro-cytochrome. Again, a low peak electric field of 0.9×10^6 V/cm is obtained at the drain end for protein as compared to other biomolecules.

Keywords*: Biosensors; InP/InGaAs/InP; Threshold voltage; Sensitivity; Dielectric Modulation.*

Investigation of TF-FinFET based Biosensor for Early Diagnosis of protein carrying diseases

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Abstract: This article deals with a comprehensive study of a FinFET based biosensor conducted on Atlas Silvaco TCAD software at 20 nm node. The implementation of a label free biosensor has been studied on the conventional as well as the truncated fin (TF) FinFET structure for early diagnosis of harmful diseases. A nanocavity introduced between gate metal and gate oxide induces an extra capacitance on immobilization of biomolecule, which ultimately alters device transfer characteristics. TF-FinFET found relatively higher switching ratio (i.e., 80 times) and lower OFF-state current (i.e., 10 times) and high sensitivity for each analysed k-value. Hence, TF-FinFET proved itself a better candidate than conventional FinFET. Moreover, further analysis of analog FOMs have been done for TF-FinFET as an evidence of enhancement. Early diagnosis for protein carrying diseases like ovarian cancer, Alzheimer's disease and coronary artery disease are possible with the help of TF-FinFET based biosensor.

Keywords*: dielectric constant; biomolecule; Biosensor; sensitivity; FinFET*

Computing Electromagnetic Bandgap for Parallel Nanorod Structure with Double Negative Refractive Index inside Triangular Lattice

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Abstract: Complete electromagnetic bandgap is analytically computed for parallel nanorod structure when placed inside a triangular lattice in symmetric fashion. Being a metamaterial or double negative refractive index material, this structure exhibits tunable bandgap when dimension of the cylinder, i.e., fill factor of the structure is changed within feasible mechanical limit. Formation of bandgap becomes only possible for magnetic polarization, whereas even quasi-bandgap is not observed for electric polarization. Maximum bandgap width is obtained for 0.45 value of normalized radius of the nanorod, and corresponding midband frequency is computed. Field patterns are also obtained for the desired frequency values. Maximum and minimum bandgap inside first Brillouin zone is calculated which plays critical role for photonic filter design.

Keywords*: Complete bandgap; Magnetic polarization; Parallel nanorod; Triangular lattice; Field pattern*

A Comparative Investigation on Characteristics of Conventional MOSFET and Ferroelectric Thin Film Modified FET

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Abstract: - In this work, we examined a new design approach of field-effect transistor with ferroelectric material layer (FE-FET) based on the theory of negative capacitance, which helps in lowering the sub-threshold swing and lift on-off current ratio with small hysteresis. The intensive investigation was performed on a conventional field-effect transistor (FET) and proposed FE-FET device. TGF, gd, Cgg, VA and short channel effect (DIBL, SS, VTH) and fT are discussed and compared. The results suggest that the proposed device can be used in ultralow power and ultralow voltage that works as a new energy-efficient device because the off current is decreased by one order of magnitude and also subthreshold swing in linear and saturation region is decreased by 7.09% and 16.86% respectively.

Keywords*: Sub-threshold swing, ferroelectric materials, negative capacitance, energy-efficient device*

Ta2O5 as Tunneling Oxide For n-type Passsivated c-Si CS-TOPCon Solar Cell

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Abstract: The Tantalum oxide (Ta2O5) as an alternating material to the SiO2 has been investigated in this. The Ta2O5 as an Anti-Reflecting coating material can also be used as the tunneling oxide material, because the electrical insulating material in the ultrathin oxide region has potential to produce extremely high electric field due to tunneling effect. The enhanced carrier transport increases the passivation quality of the designed c-Si based solar cell. It also provides the carrier selectivity because of the capacitor behaviour. The performance evaluation is done with Silvaco ATLAS TCAD simulator using ASTM certified AM1.5G globally accepted spectrum. The conversion efficiency of η=28.12% is obtained for the minimum thickness of the oxide region. The performance of the designed solar cell with Ta2O5is then compared with the basic and passivated c-Si solar cell.

Keywords*: CS-TOPCon solar cell, electric field, efficiency, ATLAS, pinholes.*

Linearity Performance Analysis of Charge-Plasma-Based Hetero-dielectric Nanotube Tunnel FET

A.Gedam[1], B. Acharya[1], & G. P. Mishra (Times New Roman 11, Bold, Italics, Left Justified)

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Abstract: The manuscript presents, linearity performance parameters for a new hetero dielectric shifted core gate nanotube structure (HD-SCG-NT-TFET) for the applications like low standby power and radio frequency ICs (RFICs). In this proposed device core gate workfunction is similar to the shell gate. The core gate provides better electrostatic controllability and also increases the turn-on capability of the nanotube TFET. In addition, the manuscript also gives a comparative analysis of high-K gate dielectric(HfO_2) in terms of gate oxide channel interface trap charge (ITCs) performed on nanotube structures. The crucial linearity parameters for low power radio frequency application of nanotube TFET structures are also investigated in terms of VIP2, VIP3, IIIP3, IMD3, and 1 dB compression point for negative, neutral, and positive ITCs.

Keywords*: Charge plasma, junctionless; core gate; nanotube ; shift core gate*

Optical XOR-XNOR logic circuits using mechanical movable

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Abstract: Using movement of mirrors mechanically one can easily create the different path for light. In this paper, we have performed three-variable XOR and XNOR logical operations using mechanical movable mirrors. It is utilized in basic computerized expansion circuits which figure the entirety and convey of two bit or three bit numbers. XOR entryways are additionally used to decide the equality of a parity of binary number, i.e., if the all out number of 1's in the number is odd or even. The XNOR rationale gates are utilized in mistake identifying circuits which are to recognize odd parity or even parity bits in advanced information transmission circuits. XNOR entryway is basically utilized in arithmetic and encryption circuits. This simple design can be easily fabricated into chip level..

Keywords*: Computing; Optical logic; Plane mirrors*

Analysing Structural Asymmetry on the Nonmonotonic Electron Mobility of Pseudomorphic Heterojunction Field Effect Transistors

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Abstract: Nonlinearity in the mobility of electron can be determined in a GaAs/$In_xGa_{1-x}As$ double quantum well pseudomorphic Heterojunction Field Effect Transistor via asymmetry in the doping concentration along the substrate side. We observe a sudden fall in electron mobility near the resonance of subband energy states which affects subband electron mobilities governed by ir-scattering. The nonlinearity in μ increases with increase in difference in the well width and doping concentration.

Keywords*: Strained double quantum well; Nonmonotonous electron mobility; InGaAs/GaAs p-HFET structures; Subband energy states*

Effect of Well Width and Barrier Width on I–V Characteristics of Armchair Graphene Nanoribbon based Resonant Tunneling Diode Structure

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Abstract: We study the effect of well width (W_w) and barrier width (W_b) on *I-V* characteristics of symmetric armchair graphene nanoribbon (AGNR) based resonant tunneling diode (RTD) structure. We show that the decrease of either W_w or W_b increases the peak current I_P. As W_w increases, I_P occurs at less bias voltage *V,* however, with the change in W_b, I_p occurs almost at the same value of *V*. The respective transmission coefficient as function of subband energy levels correlate the *I-V* characteristics. Our study indicates better results using a narrower well and thinner barrier structure anticipating the suitability of graphene for developing 2D resonant tunneling diodes for future nano-electronic devices.

Keywords*: Armchair Graphene Nano Ribbon; Resonant Tunneling Diode; Non-Equilibrium Greens Function; 2D Negative Resistance Devices*

Effect of biaxial strain on the electronic structure of Nb-doped WSe_2 monolayer: a theoretical study

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Abstract: Strain engineering is an effective strategy to tune the electronic structure of two-dimensional (2D) materials. In this work, we analyzed the effect of biaxial strain on the electronic structures of Nb-doped WSe_2 monolayer (ML) by using the density functional theory (DFT). The bandgap of Nb-doped WSe_2 ML is calculated as 1.43 eV under unstrained condition and it is an effectual p-type direct bandgap semiconductor. The formation energy calculations suggested that Nb-doped WSe_2 ML under biaxial strain varying from -5% to +5% are thermodynamically favourable under the Se-rich experimental conditions. By comparing the rate of bandgap tunability of Nb-doped WSe_2 ML, it is clear that the biaxial tensile strain is more effective in tuning the.

Keywords*: Density function theory, Tungsten diselenide, substitutional doping, formation energy, biaxial strain.*

Numerical Analysis of an Ultra-High Negative Dispersion Compensating Micro-Structured Optical Fiber with Air-holes Arranged in Octagonal Structure

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Abstract: In this paper, a high dispersion compensating photonic crystal fiber (PCF) has been proposed, fabricable with simple fabrication schemes. The lattice design structure is comprised of five rings of circular air-holes. The rings are arranged with an octagonal geometry. The fiber exhibits an ultra-high negative dispersion, that cancels the accumulated positive material and group velocity dispersion, such that the transmitted optical signal remains almost undistorted. The full vector finite element method (FEM) incorporated with a circular, perfectly matched layer (PML) at the boundary is implied to investigate the different optical properties of the proposed fiber. The numerical simulation of the designed fiber indicates that an ultra-high negative dispersion of –3112 ps.nm-1.km-1 at 1.55μm wavelength can be obtained, which can reduce the length of dispersion compensating fiber significantly. Besides, the structural diameter deviation of ±2% over the optimum value of the proposed PCF is evaluated for investigating fabrication flexibility. Moreover, the proposed fiber exhibits high nonlinearity of 94.89 W^(-1) 〖km〗^(-1)at 1550 nm wavelength, which makes the proposed fiber a suitable candidate for optical back-propagation application, super-continuum generation, and high-bit-rate optical transmission system.

Keywords*: dispersion, fiber optic transmission, non-linearity, octagonal PCF, photonics, photonic crystal fiber*

Exhibiting Dispersive Characteristics at 1330 nm for Optical Pulse Propagation through 2D Kerr Nonlinear Medium

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Abstract: Finite Difference Time Domain (FDTD) method is utilized for modelling the optical pulse propagation in two-dimensional Kerr nonlinear dispersive medium. Through our investigation, spacio-temporal propagation owing to the nonlinear effect is exhibited through modal analysis; and corresponding pulse broadening effects are displayed as a combined result of temporal dispersion and spatial diffraction. Simulation is carried out using opti-FDTD software. 1330 nm wavelength is considered for the present study, which is theoretically distortionless; however, still demonstrate the dispersive nature owing to the Kerr effect. With high intensity pumping, both TE and TM modes are plotted along with the computation for energy flow. Results are important for designing aperiodic lens and for optical switching.

Keywords*: Kerr effect; Nonlinear medium; FDTD method; Poynting vector; Pulse broadening*

Implementation of Fractional Sample Rate Digital Down Converter for Radio Receiver Applications

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Abstract: This paper briefs a novel approach of field programmable gate array (FPGA) based fractional sample rate digital down converter (FSRDDC) which reduces the sample rate from intermediate frequency (IF) to baseband frequency to meet any practical application. The proposed architecture is highly module and generic that can modify its fractional rate during run time configuration. The proposed fractional rate decimation filter allows frequency translation with a high clock rate and also performs low-pass filtering operation to ensure perfect output. The proposed FSRDDC has been tested on Kintex-7 Xilinx FPGA target device on XC7K70T-FBG676. The comparison results show that proposed scheme is superior to the other similar design in terms of less area, low power consumption and high speed, so that the design is suitable in digital radio receiver applications.

Keywords*: Fractional sample rate digital down converter (FSRDDC); Cascaded integrated comb (CIC); Digital down converter (DDC); Multi-channel systolic finite impulse response (MSSFIR); Field programmable gate array (FPGA)*

Multisubband Electron Mobility in Pseudomorphic $Al_{0.3}Ga_{0.7}As/In_{0.15}Ga_{0.85}As$ Double Quantum Well based FET Structure

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Abstract: We analyze theoretically the impact of applied electric field F on multisubband electron mobility μ in $Al_{0.3}Ga_{0.7}As/In_{0.15}Ga_{0.85}As$ double quantum well structures. We analyze μ by taking ionized impurity (*II*-), alloy disorder (*AD*-), and interface roughness (*IR*-) scatterings. It is observed that when F is applied either from the substrate (positive) or surface (negative) side of the structure, the mobility μ due to *II*- and *AD*- scatterings are symmetric as a function of F. However, μ due to *IR*- scattering is asymmetric and tilts the potential more towards the substrate side leading to more drop in μ in the case of the positive F as compared to the negative F. We also show that the reduction in the central barrier height improves μ by reducing the *II*- and *IR*-scatterings.

Keywords*: Pseudomorphic Double Quantum Well*; *Random Phase Approximation*; *Multisubband Electron Mobility*

Investigation of Work Function Variation on the Electrical Performance of sub-7nm GAA FETs

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Abstract: This paper presents the impact of work function variation (WFV) in Gate-All-Around Field Effect Transistors (GAA FETs) using the technology computer-aided design (TCAD) tool for sub-7nm high-performance logic applications. We have compared the WFV induced electrical characteristic variations in nanowire (NW) and nanosheet (NS) GAA FETs. We study the impacts of different grain sizes on the performance of NSFET and NWFET using statistical data analysis. The variation in critical electrical figures-of-merit (V_{TH}, I_{ON}, I_{OFF}, SS, and DIBL) have been analyzed. It is predicted that the NSFET shows improved immunity toward V_{TH} variation than NWFET. Overall, the NSFETs are less prone to performance variations compared to NWFET. As such NSFET architectures will be the preferred choice for logic devices below sub-7nm technology nodes.

Keywords*: Gate-all-around (GAA) FET, Nanowire, Nanosheet, Work Function Variation.*

Enhanced DC Performance of Junctionless Field-effect Transistor Using Dielectric Engineering

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Abstract: In this paper, a simulation study of a novel structure of Double Gate Junctionless FET (DG-JLFET) having Dielectric Pockets inside the channel region is being reported for the first time. Based on 2D TCAD simulation results, it is observed that the proposed structure not only wanes the OFF-state current but also improves the current switching ratio by avoiding any degradation in the ON-state current. A significant reduction in the penetration of the lateral electric field into the channel is found to cause a notable reduction in the OFF-state current in the proposed device. The proposed device provides flexibility in terms of optimizing and enhancing the performance parameters of DG-JLFET by varying thickness and width of the Dielectric Pockets (DPs). A new scope of research and development lies in the newly proposed structure of the DGJLFET incubated with Dielectric Pockets located between the two gate oxides.

Keywords*: Current-switching ratio; Dielectric Pocket; Junctionless Field Effective transistor*

DG MOSFET for Bio-Sensing Applications: A Review

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Abstract: The research and use of FET for biomedical application has increased and found its usage as a biosensor for the detection of biomolecules. Detecting various diseases like pathogens, cancer, viral diseases has been difficult and time taking. Using FET as a biosensor for identifying different biomolecules has been a less costly and time-saving process and can also be used in detecting diseases at an early stage. Mass production of FET's is very cheap as compared to the different other devices like nano-mechanic, piezoelectric, optical etc. which are very expensive. In this paper, different device structures are shown that are used as a biosensor to detect biomolecules of different dielectric constant.

Keywords: *MOSFET; biosensor; biomolecules; double gate ; junctionless*

A Hetero-Dielectric Double-Gate Junctionless FET with Spacer for Improved Device Performances

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Abstract: In this paper, we lay out a simulation study of DC parameters for a hetero-dielectric junctionless field transistor along with the best possible combination of high-*k*/low-*k* spacer dielectric on both ends of the gate oxides of the device. Various parameters, such as ON-current, subthreshold leakage current and current switching ratio are analyzed and compared with single-material gate (i.e. conventional) DG-JLFET. A significant improvement in the current switching ratio is observed for the presented device when the length ratio of two gate oxides is kept at an optimum value with high-*k* and low-*k* spacer on source and drain end, respectively. It is mainly attributed due to the fact that different spacer and gate dielectric introduced at both the ends alters the fringing electric field along the channel, mainly at channel-drain interface, and eventually reduces the OFF-state current by at least 100 fold as compared to that of SMG-JLFET.

Keywords*: Current-switching ratio; DC parameter; Junctionless Field Effective transistor; hetero-dielectric*

Impact of Channel Engineering on 16nm, 18nm & 20nm Doping-less DG MOSFET S

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Abstract: Double Gate MOSFET is a promising candidate for future low power applications with low leakage current and increased gate control over the channel electric field. Double gate MOSFET (DG-MOSFET) are designed as symmetric and asymmetric architectures with different gate overlap or underlap regions to achieve better subthreshold performance. The channel analysis on double-gate MOSFET shows that low channel doping with equal dopant atoms as in source and drain is a suitable choice to keep leakage current smaller and a suitable threshold voltage change. Subthreshold performance parameters are considerably improved with the concept of low doping junction-less double-gate MOSFET. High-K dielectric material (HfO_2) with high work function gate contact material as platinum is also a suitable choice to achieve low leakage current. Channel doping is helpful within the context of leakage power reduction, thus in optimizing the device parameter the channel doping can contribute the necessary role. The proposed DG-MOSFET is designed and analyzed on a Visual TCAD 2D and 3D device simulator.

Keywords*: DG-MOSFET, DIBL, Visual TCAD, Short channel effects, Nano Regime, Channel doping.*

Recessed Channel Carbon Nanotube Truncated Fin Finfet For High Performance ULSI Applications

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Abstract: In this work, carbon nanotube (CNT) channel based recessed channel (RC) truncated fin (TF) FinFET has been presented and compared to a simple truncated fin (TF) FinFET and recessed channel truncated fin (RCTF) FinFET on the basis of their corresponding Switching Ratio (102 and 103 times enhancement respectively), 1-dB Compression point, Intrinsic gain (with 42.8% enhancement), VIP3, IMD3, and other transfer characteristics. All the simulations of concerned devices have been performed with the help of Silvaco Atlas tools at 7 nm gate length. Moreover, because of these enhancement in RC and RC-CNT-TF-FinFET, one can predict the optimization in transfer characteristics for high density circuitry performance if seen from the perspective of ULSI applications.

Keywords*: Recessed channel, TF-FinFET, RC-CNT-TF-FinFET, linearity, analog*

Novel SPICE Model for bifacial solar cell to increase the renewable power generation

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Abstract: The Novel SPICE Model for bifacial solar cell to increase the renewable power generation is presented in this paper. The performance of the model for bifacial illumination new bifacial parameters are measured using a spice model using one-diode model of the PV module. The conventional system is very costly, time consuming and bulky, so a simulation system is needed to do more research for optimal results. In this research studies a simulation of spice model is presented through which a behaviour of bifacial solar cell is predicted. The outcomes displayed close to straight varieties of boundaries of interest with apparently decreased reaction time. This methodology depends on the SPICE model. The efficiency of the bifacial solar cell module is found to be 9% more than the conventional model consuming a very low power in the order of 9 µW. The advancement of SPICE model for bifacial solar cell is novel which is quick in activity and easier to understand. The simulation has been done on Tanner Tool simulator version 16.3 for a 70 nm process model.

Keywords: *SPICE, sensor, bifacial solar cell module, short circuit current, open circuit current.*

Body Connection Assessment of MOS-Diodes for MOS-Quadrupler based RF Energy Harvesting Circuit

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Abstract: In this paper, we present a highly sensitive RF energy harvesting circuit which utilizes MOS-Quadrupler as rectifier and a passive series resonance circuit that acts as a voltage booster as well as a matching circuit. For rectification of RF signals, we have used MOS-diodes with body-drain connection instead of widely used body-source connected MOS-diode (conventional). The proposed circuit is designed and optimized for 900 MHz (ISM Band) frequency using standard 90 nm CMOS- technology. We achieved the power conversion efficiency (PCE) 36% @ - 30 dBm and 1V - sensitivity at - 25.6 dBm for 1 MΩ load. The achieved PCE is 39.5% higher than the conventional MOS-diode (body-source) rectifier at a remarkably low RF input power of -30dBm (1 μW) due to reduction in leakage and enhancement of charging current.

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Keywords: RF energy harvesting; Passive voltage boosting; Rectifying device.

Capacitive analysis of Strained Superjunction Vertical Single Diffused MOSFET

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Abstract: This paper, provides a discussion on area specific input capacitance of Strained superjunction vertical single diffused MOS (s-SJVSDMOS). Workfunction engineering is applied to the device. With the help of workfunction difference, doping of source, drain and body region is bypassed in the structure. To form the strain region SiGe is employed. To perform the capacitive analysis an AC signal is applied at the gate to source terminal and the area specific input capacitance of the device is obtained. The switching capacity is studied using the gate charge curve. The observation was performed for three different width of the strained layer.

Keywords*: Power devices; gate charge; area specific on resistance ; input capacitance, superjunction, VDMOS*

Performance Analysis of FinFET based inverter at 7nm Technology Node Using TCAD Simulation

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Abstract: In this work, a layout-based FinFET design approach has been presented at 7nm technology node. Using Technology CAD (TACD) physic based tool, the electrical performances have been investigated for both n and p-channel FET. A mixed-mode integrated simulation environment has been implemented to realize the CMOS inverter for circuit applications. The signal propagation across the designed inverter has been investigated. The improvement in maximum power (Pmax) performance and switching energy behaviour can be observed with variation in drain voltage and fin height.

Keywords*: FinFET; CMOS; inverter layout; DG Model; TCAD tool*

Computational analysis of doped (10, 0) MoS2 ANR metal junction by Schottky Barrier height modulation

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Abstract: In this work, we have experimented the effect of substitution in MoS_2 armchair nanoribbon (ANR) metal junction. Ab-initio calculations and Non equilibrium Green's function (NEGF) simulation methodologies are used here. Various contact metals like Titanium (Ti), Chromium (Cr), Aluminum (Al) and Silver (Ag) are used for our experimentation. Important electronic properties like bandgaps, carrier effective masses and variation of work function variations were calculated with help of Density Functional Theory (DFT). Further with the Schottky-Mott formula we evaluated the Schottky barriers and the currents is measured with NEGF calculations. Experimental results gives further scope of improvement of current with modulation of Schottky barrier height when proper substitution and contact material combination is used.

***Keywords**: MoS_2, nanoribbon, substitution, Schottky barrier height.*

Influence of High-k Dielectrics on Nanowire FETs

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Abstract: In this work, design optimization of Nanowire Field Effect Transistor (FET) has been carried out for switching applications. The reported device offers an increase of 122 µA in drive current as compared to the device with SiO_2 as a gate oxide and I_{on}/I_{off} ratio of 10^7. The threshold voltage (V_{th}) is 0.35V with Drain Induced Barrier Lowering (DIBL) of 60.52 mV/V and Subthreshold Swing (SS) of 72.04 mV/Dec. The off-state leakage (I_{off}) is 103.75 pA which is 71.67 pA higher than SiO_2 based device but can be traded-off with an increased drive current of 161 µA and transconductance of 642.78 µS in HfO_2 based device making it suitable for digital logic applications.

***Keywords**: Nanowire, High-k, Interface Charge, Digital Logics*

Nanocomposites based Solid State Electrochromic Nano-Material Membrane Device

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Abstract: Electrochromic Nano-Material Membrane (ENM) Device is developed on ITO coated glass substrate. The device comprises of nanocomposites such as WO3 doped Ag NW, H doped Nb2O5 and PEO which appeal considerable attention for their application in advanced window and smart display. The device is fabricated with a set of carried nanocomposites using Sputtering process. For colouration and bleaching state the transmittance and optical modulation of ENM device is contrasted with existing Electrochromic Devices and is found to be 8.6-52.6% transmittance modulation enhancement in the visible spectrum. The switching time of the ENM Device is found to be 107sec, which implies augmented performance of ENM in advanced technological applications.

Keywords*: Nanocomposites, Nano-Material, Transmittance, Optical Density, Switching Time*

Autonomous Remote-monitoring Low-cost Agricultural System

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Abstract: The growing world population requires the maximization of food production per unit area. A vertical system can meet this need. This technique uses stacked grow beds with artificial lighting and an automatic irrigation system to significantly eliminate water and nutrient loss. The addition of polyhouse to the system makes it possible to grow factories at high altitude, thereby minimizing transportation and overall cost. this system are often wont to produce most sorts of crops, from ornamentals to high altitude plants and grasses. The extensive recycling of nutrients makes the implementation of this agricultural technique sustainable and profitable. it's perfect for the urban population where agricultural land is shrinking and therefore the scarcity of beverage is increasing day by day.

Keywords*: Vertical farming; polyhouse; nutrient recycling; water conservation; food*

Power Supply Noise Aware Physical Design with Decoupling Capacitance Allocation in System-on-Chip

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Abstract: Reduction of switching noise is a major challenging task in today's system-on-chip design. The supply noise occurs in the pad locations due to inductive effect, resistive loss occurs due to electrical wiring on the chip and is also an effect of high switching activity of the transistors. This variation in voltage in the various electrical nodes may result in functional failure of the integrated circuit. Use of decoupling capacitors is a commonly used technique to reduce the power supply noise. Estimation and allocation of decoupling capacitors is a challenging task in the design process. Thus a lot of effort has to be given in the physical design stage to improve the overall performance of the integrated circuit. This article presents computer aided design approach to estimate decoupling capacitor and placement at the physical design stage to reduce the power supply noise. The main focus of this work is on allocation of decoupling capacitors so as to reduce the supply noise and also to keep cross-sectional area at its best after allocation of decoupling capacitor. Simulation results shows the overall design parameters are also satisfactory. This technique can also be used in other system-on-chip design.

Keywords*: Ant Colony Optimization (ACO), Computer Aided Design (CAD), Decoupling Capacitor (decap), Particle Swarm optimization (PSO), Power Distribution Network (PDN).*

A Low Voltage Rectifier for Piezo-Electric Energy Harvesting Designed in CMOS Technology

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Abstract: A low voltage pMOS based rectifier with moderate power conversion efficiency (PCE) for harvesting of Piezo Electric energy is presented in this work. The topology is achieved by utilizing the pair of pMOS devices with their gate terminals cross coupled in addition to another pair of pMOS transistors diode connected whose body terminals are tied to their own well. Based on standard 45nm CMOS technology, the simulations for the proposed work are performed in Tanner T-SPICE. Comparison of the proposed work with other existing topologies are also performed which shows VCE is close to 44.5% and 43.1\% respectively, for an input voltage equals to 1Vp-p, 100kHz with load resistance 10kΩ and capacitor of 150nF.

Keywords*: Energy Harvesting, Piezo-electricity, Rectifier*

A Design of Frequency Encoded Dibit-based Comparator Using Reflective Semiconductor Optical Amplifier with Simulative Verification

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Abstract: In this modern era, optical computing increases the chance of ultra-high-speed information processing. All-optical comparator is one of the necessary components of the optical computing systems. Here, we have designed a low power frequency encoded comparator using reflective semiconductor optical amplifier. This proposed comparator can compare a single bit signal. This work is based on dibit concept which improves the bit error problems. The proposed comparator is realized by simulation in MATLAB Simulink (R2018a) software. The devised design with the integrating ability is very purposeful in optical communication and computation.

Keywords*: Optical Communication; Dibit-based logic system; Frequency encoding; Reflective semiconductor optical amplifier; Comparator.*

Power optimized 10 bit ADC design in circuit level

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Abstract: In this research work a 10 bit SAR(Successive Approximation Register) type ADC(Analog to Digital Converter) IP(Intellectual Property) has been approached with some specifications along with the circuit diagram of each elementary design block. Here 180 nm technology has been used. Various types of performance parameters like area, resolution, i/p current, i/p impedance, conversion time etc. have been discussed. Also the pre-layout as well as post layout simulation results have been given in this paper.

Keywords*: Analog to Digital Converter; Successive Approximation type Register; circuit level*

A non-iterative hybrid dynamic state estimation scheme utilizing PMU and SCADA measurements

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Abstract: In this paper, a novel hybrid dynamic state estimation technique (NHDSE) has been proposed for estimating power system states which are primarily bus voltage magnitudes and phase angles at each bus. The proposed NHDSE utilizes a suitable linear relationship existing between measurement and states. Thus, the filtering purpose has been resolved through dynamic state estimation (DSE) approach based on linear Kalman filter rather than popularly used Extended Kalman filter (EKF). With the utilization of linear scheme, the proposed approach is iterative free and thus the observation matrix is calculated only once at the beginning. The proposed scheme is compared with conventional EKF based DSE. In order to corroborate the efficacy of the proposed approach, the same has been applied on two IEEE systems i.e., IEEE 14 and 57 bus test system. Obtained results clearly show the efficacy of the proposed scheme.

Keywords: *NHDSE; linear Kalman filter; filtering; iterative free; conventional EKF.*

MODELING AND SIMULATION OF GaAs NANOWIRE TRANSISTORS

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Abstract: This project is to study about characteristics of nanowire transistor. The simulation is done by SILVACO software to find the characteristics of nanowire transistors. Here simulation is more important to understand the device physics and performance limits of the nanowire transistors. By the support of the simulation tools experimental work can be done for nanowire transistor. With the help of simulation, we can know the weakness and strength of nanowire transistors. That will help to reduce the fabrication cost. As we go for the smaller size for the transistor then nanowire transistor comes into the picture. For electronic device Silicon, Germanium and Gallium Arsenide semiconductor materials are generally used. Here production of Silicon simple as compare to Gallium Arsenide but when high speed device is required then we go for Gallium Arsenide material.

Keywords: *nanowire transistors, simulation, electrostatic gate control, device*

Influence of high-*k* oxide thickness on gate stack DMG junctionless SOI MOSFET

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Abstract: The present paper describes the influence of Gate stacking on Dual Material (DM) Junctionless (JL) SOI MOSFET operating in Junction Accumulation Mode (JAM). The performance of the proposed MOSFET structure, simulated with 2D ATLAS device simulator, is investigated for variations in thickness of the high-*k* (HfO_2) Gate oxide. The analog performance of the DMG JL JAM SOI MOSFET is examined on the basis of its transfer characteristics, transconductance, transconductance generation factor, Drain induced barrier lowering(DIBL), I_{ON}/I_{OFF} ratio and gate capacitance variations with the gate voltage. Its cut-off frequency is also studied. In addition, a single stage amplifier based on the proposed MOSFET is simulated and its response is studied for the variations in high-*k* oxide thickness. The simulation results reveal that reduction in the high-*k* oxide thickness improves the device performances.

Keywords: *DMG JL JAM SOI MOSFET, DIBL, High-k, HfO_2*

Temperature associated reliability analysis of a Si/Ge Heterojunction Dopingless Tunnel FET Considering Interface Trap Charges

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Abstract: This manuscript investigates the effect of variations in temperature and interface trap charges (ITC) on the analog and radio-frequency (RF) performance parameters of a Si/Ge heterojunction (HJ) asymmetric double-gate (ADG) dopingless (DL) tunnel field-effect transistor (TFET) with high-κ gate dielectric and abbreviated as HJ-ADG-DLTFET in the manuscript. The HJ-ADG-DLTFET makes use of small bandgap source material (i.e., Germanium (Ge)) instead of silicon (Si). Consequently, increment in band-to-band tunneling (BTBT) and hence drain current flowing across source-channel tunneling junction, due to Si channel. The simulation is done by utilizing Silvaco ATLAS device simulator at various ITC density and polarity and, for a broad temperature spectrum from 200 – 400 K. The results illustrate that higher PITC (Positive ITC) density degrades device performance enormously. Furthermore, temperature variations for the range from 200 – 400 K demonstrate the degradation of the off-state current for HJ-ADG-DLTFET.

Keywords: *doping less; interface trap charges; reliability; temperature; tunnel FET*

Novel 9:1 Ternary Multiplexer on 32nm CMOS Technology

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Abstract: Present study explores new 9:1 Ternary-Multiplexer (T-MUX) using Normal Process Enhancement-type Metal Oxide Semiconductor (NPE-MOS) transistors without any threshold modifications. The 3:1 T-MUX based on proposed idea is designed first and that has been exploited in order to design the proposed 9:1 Ternary Multiplexer next. The front end circuit-design and optimization of proposed Ternary Multiplexer is performed on 32nm standard CMOS technology using BSIM4 device model with 1.0V supply rail at 27°C temperature. Ternary-digits "0", "1" and "2" are presented with 0V, 0.5V and 1.0V respectively. The designed circuit has been validated through extensive T-Spice simulations with all possible test patterns. As per evaluation the proposed 9:1 T-MUX consumes 51.37µW average power when operated with 3.2GHz of selection speed. The propagation delay of proposed circuit becomes 15.07ps.

Keywords*: Enhancement-type MOSFET; Pass Transistor Logic (PTL); Power-Dissipation; Multiplexer; Ternary Number System*

DC Exploration of Oxide Trap Charge Effects on Electrically Doped Nano Ribbon FET

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Abstract: Most next-generation transistors are based on the concept of multi-gate structure. These devices have to be designed with more number of gate insulator layers than the planar transistor. Hence, the chances of trapping of charges in the oxide and interface region is more than the conventional designs. So we consider the Nano Ribbon Field Effect Transistor (NRFET) to analyze the trap charge effect on the DC characteristics. The analysis has been done based on input characteristics and off-state current along with the transconductance and TGF. The effect of temperature on the oxide trap was also verified in terms of threshold voltage changes for the considered device. The complete analysis has been done on the Visual TCAD device simulation tool.

Keywords*: gated resistor, electrically doped, multigate FET, trap charges*

Robust Design of Noise Tolerant 2-Phase Non Overlapping Clock Generating Circuit

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Abstract: This paper presents a circuit level technique for designing a robust 2-phase non overlapping clock generating circuit. The proposed 2-phase non overlapping clock generating circuit is simulated with Monte Carlo simulation sweep of 5000 and at a frequency of 1.5 GHz. An extensive simulation of the proposed circuit is performed using 16-nm high performance predictive technology mode (PTM) on SPICE platform. The proposed technique is observed to have high average noise threshold energy (ANTE) compared to the conventional circuit by a factor of 1.43X and also mitigating the impact of process, voltage and temperature variations, on various design parameters such as propagation delay, average power and power-delay product. The proposed circuit exhibits an improved noise characteristics and variability compared to the conventional circuit by using a 4-transistor based Schmitt trigger in place of inverters.

Keywords*: ANTE; Variability; 2-phase NOCG; Schmitt trigger.*

AlGaN/GaN HEMT with Recessed T-Gate and Floating Metal for High Power Applications

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Abstract: This paper presents a millimeter-wave wide bandgap material AlGaN/GaN heterojunction FET, also known as HEMT (high electron mobility transistors) for high frequency and high-power applications. This work employs the technique of recessed T-gate, which reduces gate resistance, helps to improve power consumption by reducing SCEs (short channel effects) and consists of floating metal with triple teeth (TT) located inside the buffer layer. The obtained f_T and f_{MAX} are 101 GHz and 530 GHz at V_{DS} = 10 V with V_{GS} = 0.4 V, respectively. Output power of 67.5 dBmW with power gain of 11.6 dB and power-added efficiency of 24.6% at V_{DS}= 30 V, Continuous Wave at 10 GHz. The theoretical model of the device has been verified with the simulated results obtained from Atlas of Silvaco.

Keywords*: HEMT; Transconductance; Cut-off frequency; Power gain; Power-added efficiency.*

An ab-initio study of 2 dimensional metal (Cu, Ag) - 1T' ReS2 van der Waals heterostructure

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Abstract: In this work with density functional theory calculations, we investigated the van der Waals heterostructure (vdWh) between metallic 2 dimensional (2D) sheets of Cu and Ag with monolayer 1T' ReS2. With structural relaxations inclusive of van der Waals forces, the stable interfacial configuration were optimized. Thereafter the various properties of the vdWh, such as density of states, electron density, total potential and electron localization function, were thoroughly investigated. The computational studies show that both the heterostructures display a metallic to semi-metallic nature, with the Cu-ReS2 structure being more metallic. In terms of electrostatics, a larger concentration of electrons were observed on Cu as compared to Ag for the two interfaces, while an electron gas like feature could be seen between the 2D Ag and ReS2 layers. The results are of interest for 2D nanoelectronics devices and flexible electronics applications.

Keywords: *Density functional theory; 2D materials; van der Waals heterostructure*

TCAD Analysis and Simulation of Double Metal Negative Capacitance FET (DM NCFET)

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Abstract: In this paper, we investigated Double Metal Negative Capacitance FET (DM NCFET) for improved digital and analog performance in comparison to the conventional Negative Capacitance FET(NCFET) by using a new concept of Ferroelectric layer (HfO2FE). Visual TCAD software is used to make a proposed device DM NCFET. The results have been analysed in form of leakage current (I_{off}), Transconductance (G_m), Transconductance generation factor(TGF),Early Voltage (V_{EA}),Intrinsic gain (A_v), Unity gain Cutoff Frequency (f_T) and improved the performance of output conductance (G_d), drain barrier induced lowering (DIBL), Switching ratio I_{on}/I_{off}, Subthreshold Swing (SS).Thus, DM NCFET can be suitable for digital and analog circuit applications.

Keywords: *Visual TCAD, DM NCFET, SS.*

Impact of Ferroelectric Oxide Layer on Palladium Silicide Source Electrode based Double-Gate Junctionless TFET

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Abstract: The Double-Gate (DG) Tunnel Field Effect Transistor (TFET) is widely considered to be the most important emerging device for high-performance computing applications. These devices have proven their ability to achieve the most important requirement of semiconductor industries such as low subthreshold swing (SS< 60 mV/decade) due to utilization of Band-to-Band Tunneling (BTBT) as a switching mechanism. However, the performance of DG-TFETs is limited to high thermal budget on account of the heavily-doped source and drain region. Although, charge-plasma based Junctionless (JL) device is the alternative solution for a low-thermal budget, but, the combined structure i.e., DG-JL TFET is limited to low I_{ON} along with large subthreshold swing (SS). Therefore, in this work, we have combined the three techniques such as DG, charge-plasma and ferroelectricity in order to achieve better electrostatic control, low thermal budget and low SS (< 60 mV/decade) respectively. In order to form negative capacitance in DG-JL-TFET structure, a ferroelectric oxide layer i.e., $PbZr_xTi_{1-x}O_3$ ($0.1<x<1$) has been introduced with the control gate silicon dioxide (SiO_2) layer. The reported device with the control-gate dielectric stack materials has been found to exhibit low SS of 49.9 mV/decade, switching ratio of 0.75×10^8 and the threshold voltage of 0.62 V at the supply voltage of 1 V. Silvaco ATLAS tool has been used in the present piece of work for getting out the simulations. The present findings may help to overcome the aforementioned challenges of DG-JL-TFET and thus, the reported device may be used for low-power logic applications.

Keywords: Tunnel FET, Ferroelectric, Subthreshold Swing, Charge Plasma, Junctionless

Nanowire texturisation of Multi Crystalline Silicon using Silver Assisted Chemical Etching

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Abstract: The present article describes the process of Metal Assisted Chemical Etching to produce a nanowire structure on the multicrystalline silicon surface by using silver metal catalyst. From the surface morphology (SEM) it has been observed that the produced nanowire structure of diameter ≈ 10 nm and having average length of 80 nm and 100 nm approx. has been formed for the process time 60 seconds and 120 seconds respectively. From the reflectance measurement it has been observed that the silicon nanowire provides a degree of reflectance of 5% to 8% over a spectrum range of (300 to 1000) nm.

***Keywords**: Multicrystalline, Nanowire, Nanoporous, Chemical Etching, Silver.*

Magnesium Silicide Source Double Palladium Metal Gate TFET for Highly Sensitive Hydrogen Gas Sensor

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Abstract: This work reports the application of novel magnesium silicide (Mg_2Si) source heterojunction double gate tunnel field effect transistor with palladium (Pd) gate metal for highly sensitive hydrogen gas sensor. The impact of hydrogen gas pressure on sensor is considered by change in the workfunction of palladium gate metal as a function of hydrogen gas pressure. Heterojunction formed by Mg_2Si (source) and silicon (channel) at the source-channel interface in the gas sensor under consideration compensates for the low ON currents of conventional TFET devices. All the simulation results are obtained from Silvaco atlas TCAD simulator. Investigations reveal that the behavior of proposed sensor is reasonably sensitive to the hydrogen gas as it displayed a wide range of sensitivity from the order of 10^3 to 10^7.

Keywords: *Hydrogen, gas sensor, palladium, magnesium silicide, heterojunction*

Analysis of Static Noise Margin of 10T SRAM Using Sleepy Stack Transistor Approach

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Abstract: The latest electronic gadgets demand many functionalities which requires enhanced performance of the processor. To ensure this, cache based on Static Random Access Memory (SRAM) is a vital part in electronic devices. Above 90 nm technology, we can build an SRAM in CMOS LSI technology without electrical stability, by connecting six transistors. However, leakage and variability of transistors in SRAM cell have become dominating factor below 90nm technology. So we must design SRAM bit cell with utmost care. Recently SRAM cells have been designed to deal with these problems. However, it is an important task to achieve a balanced performance between all SRAM cell parameters of sub-nanometer technology. A new design of SRAM is presented in this paper to elevate the performance. The proposed SRAM is designed and implemented in CMOS 90nm technology and produces comparatively better performance in terms of Static Noise Margin (SNM), stability and power dissipation when compared with conventional 6T SRAM. The cell reduces the energy consumption by using the technique of stacking. The stability of proposed SRAM is also high compared to recent designs.

Keywords*: SRAM, Sleepy stack, 10-T, SNM, Power consumption*

Band Offset Dependent Performance Analysis of SnO/mc-Si Heterojunction Solar Cell

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Abstract: In this paper, p-type SnO/n-type multi-crystaline silicon (mc-Si) heterojunction solar cell is studied by using TCAD simulation where SnO act as an absorber layer. Experimentally evaluated absorption coefficient of thin SnO layer is used in the simulation. Tuning of band gap which depends on growth kinetics oxygen pressure and electron affinity of SnO is considered to obtain best possible performance of the device. Results show that the power conversion efficiency of the device greatly depends on the valance and conduction band offsets between Si and SnO layers. Maximum efficiency approximately 8.523% is observed by proper selection of the band offsets without changing the device structure.

Keywords*: SnO; Absorber; heterojunction; electron affinity; band offset; mc-Si; thin film*

Temperature Variation Analysis of SiGe Source based Heterojunction Tunnel FETs

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Abstract: This paper presents a tunnel field effect transistor (TFET) as an alternative to suppress the effect of temperature on device performance. The device used is SiGe-based heterojunction TFET with a hetero-dielectric buried oxide layer. We have analyzed the device with a temperature variation from 200 Kelvin to 400 Kelvin. The device parameters analyzed are Energy bandgap, ON current, OFF current, subthreshold swing, and I_{ON}/I_{OFF} ratio. From the results obtained, it can be established that the OFF current strongly depends on the temperature, while the ON current is weakly dependent on the temperature. However, a higher ION/IOFF ratio has been maintained with the highest and lowest values achieved as 7.53×10^{13} and 1.9×10^{7} at an ambient room temperature (T = 300 K), and the minimum and maximum values of the subthreshold swing obtained are 19.5 mV/decade and 58.3 mV/decade, respectively. The results achieved have been compared with the homojunction TFET device at the same device parameters. All the simulations have been carried on the licensed version of Visual TCAD.

Keywords*: Tunnel FET; subthreshold swing; I_{ON}/I_{OFF} ratio*

Validation of Input/output characteristics of Symmetrical Double Source TFET device

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Abstract: Double Source SOI Tunnel FET (DSS- TFET) of both n and p-type has been proposed and influence of various parameters on the efficiency of the device have been analyzed rigorously and optimized using Silvaco-Atlas. The proposed DSS-TFET has been designed in such a way that by suppressing the ambipolar current, complementary performance can be achieved. The DSS-TFET has almost equivalent SS for different channel lengths. Hence, during circuit designing, 13nm n- type TFET and 5nm p-type TFET can be utilized which results in chip area reduction. As SOI architecture is used, ambipolar conduction has been improved, results in higher I_{ON}/I_{OFF} ratio of. value 10^{13} and 10^{12} for both n and p type respectively.

Keywords*: DSS-TFET; Subthreshold Slope (SS); SLIVAO- Atlas; I_{ON}/I_{OFF} ;Chip area; SOI.*

Trapezoidal Channel Double Gate Tunnel FET Suitable for better Scalability, Speed and Low Power Application

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Abstract: The performance of a double gate TFET with trapezoidal shaped channel has been analyzed in this article. The proposed trapezoidal shaped double gate TFET (TDG-TFET) provides a better ON to OFF current ratio (I_{ON}/I_{OFF}) as well as an improved subthreshold swing (SS) in comparison with a conventional TFET. The performance analysis of the proposed TDG-TFET has been achieved by varying different important device parameters such as oxide thickness, drain voltage (V_{DS}), channel length, gate work function and oxide thickness. For simulating purpose, SILVACO ATLAS has been considered. It can be observed that the achieved I_{ON} /I_{OFF} and SS is 10^{13} and 23mv/decade at V_{DS} 0.5V.

Keywords*: low power; TDG-TFET; Subthreshold swing (SS); TFET; I_{ON}/I_{OFF} ; Electric-Field; Potential.*

A New Study on Junction Temperature Management of White PCLED at High Ambient Temperature in Industrial Environment: An Indian Perspective

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Abstract: Now a day in our daily indoor-out door applications as well as industrial applications the semiconductor lighting system i.e., white PCLED has become very cheap and reliable solution. We have come across along journey where we start replacing incandescent lamps, and fluorescent lamps by LEDs, But, its main drawback is junction temperature rise while operating in high ambient temperatures like in hot mills, furnace rooms etc. and several industries where temperature fluctuates above 100°C. The light output of white PCLED in such places gradually degrades fast, as junction temperature increases with prolonged application of high ambient temperature. This study demonstrates a new method where the junction temperature is monitored by changing the width of quantum well i.e., $In_yGa_{1-y}N$ layer of semiconductor part i.e., $GaN/Al_xGa_{1-x}N/In_yGa1_yN$ of white PCLED. The simulation is done using Silvaco ATLAS-Device Simulation Software while considering a high range of ambient temperaturei.e.100°C to 223°C.

Keywords*: junction temperature, White PCLED, well width, quantum well, Chromaticity shift*

Work-Function modulated GAA MOSFET for Improved Electrostatic Controllability in Lower Technology Node

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Abstract: In a continuous effort to keep the Moore's law alive in lower technology node without deteriorating the device performance, several device engineering techniques are introduced. These engineering techniques involve channel engineering and gate metal engineering also. Evolution of Multi gate MOSFET devices from conventional planar structure to gate all around (GAA) is continuously going on. With unique design, GAA MOSFET is measured as one of the best device for better electrostatic control. The threshold voltage of a device depends on the work function of metal gate electrode. This work introduced a linearly modulated work function (5eV-4eV) metal gate along z-axis. This work demonstrates the advantages of work function modulated metal gate on the DC performance characteristics in lower technology nodes. An improved drain current (Id) with lower threshold voltage (Vth) indicates the superiority of the device for future generation applications.

Keywords*: Semiconductor; Nano; MOSFET; GAA; Work function.*

HeartHealth: An Intelligent Model for Multi-Attribute Based Heart Condition Monitoring using Fuzzy-TOPSIS Method

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Abstract: Cardiovascular infections (CVDs) are the number 1 reason for death around the world, taking an expected 17.9 million lives every year. CVDs are a gathering of issues of the heart, veins which incorporate coronary illness, cerebrovascular infection, rheumatic coronary illness, and different conditions. In this work, we used a multi-criteria-based Technique for Order of Preference by Similarity to Ideal Solution (TOPSIS) to permit compromises between rules, where a weak outcome on one basis can be invalidated by a decent outcome in another rule. This gives a more practical type of display than non-compensatory strategies, which incorporate or reject elective arrangements dependent on hard cut-offs. This results in a weighted approach from different sources of the correct value and measures the ideal distance from our subject's heart condition. For the different sources, we have used feature weights computed using PCA, LDA, and Permutation Feature importance over the Cleveland Heart dataset and used those for generating the TOPSIS model.

Keywords*: IoT; Multi-Criteria Decision Making;Fuzzy TOPSIS*

Performance Evolution of the $GaAs_{1-x}Sb_x$ FinFET for the Mole Fraction Variation

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Abstract: In this paper, impact of the mole fraction variation in device performance of III-V material based $GaAs_{1-x}Sb_x$ – FinFET has been investigated. Mole fraction variability influence the physical property of the compound material and hence significantly affect the performance of the device. Device electrical property such as electron density and mobility variation has been studied as a function of mole fraction. In addition to that device DC performance such as I_{ON}/I_{OFF} ratio, transconductance, threshold voltage and device node capacitance e.g. C_{gg} and C_{ds} have been also investigated with the help of a TCAD simulator. Simulation results claim that mole fraction could be a deciding factor for III-V ternary material for the low and high performance circuit applications.

Keywords: *III-V material, GaAsSb, FinFET, LDD, mole fraction*

SIC-TPG for path delay fault detection in Scan based BIST

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Abstract: The advent of deep submicron technology led to growing complexity of circuits and an increase in the design speed, making delay testing necessary for determining correct circuit behavior. Observation of path delay faults requires propagation of transitions in a circuit which is done by application of pair of patterns. This paper proposes a single input change test pattern generator (SIC- TPG) that creates SIC pairs and hence can be used for path delay fault detection. The same TPG also senses stuck-at faults in circuits. A path definition file is specified for benchmark circuit and mentor graphics Fastscan tool is used to obtain the fault coverage. For the purpose of area overhead comparison, the TPG is coded in verilog and simulated by Xilinx ISE simulator and improved results are observed. Experiments conducted on ISCAS-85 and ISCAS-89 benchmarks show high stuck-at fault coverage and Path Delay Fault (PDF) coverage.

Keywords: *SIC-TPG; Low power BIST; Path delay faults.*

Simulation and Performance Analysis of novel InN-GaN-BTG-MOSFET

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Abstract: The paper presents a numerical simulation of novel Indium Nitride and Gallium Phosphide based GaN-BTG (Buffer Trenched Gate) MOSFET. The electrical characteristics such as Transfer characteristics, Transconductance, Electron mobility of InN-GaN-BTGMOSFET and GaP-GaN-BTG-MOSFET are exhaustively analyzed using the Atlas TCAD tool. A comprehensive study is presented comparing the InN-GaN-BTG-MOSFET with GaN-BTG and GaP-GaN-BTG MOSFETs in terms of their performance characteristics. An improvement of 60.48% in SS and an increment of 47.16% in the electric field is observed which is because of the appliance of GaP and InN in the GaN-BTG structure. InN-GaN-BTG-MOSFET proves to be a promising structure to obtain enhanced performance for sub-20nm transistors and may be used for further scaling up the device.

Keywords*: Gallium Phosphide, Indium Nitride, GaN-BTG-MOSFET, Gate stacking*

Lower Fin Dimension Modulation Analysis for a Novel 5nm Top Bottom Gated Junctionless FinFET for improved performance

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Abstract: In this paper, lower fin dimension modulation is performed for a Novel 5nm Top Bottom Gated Junctionless Fin shaped Field Effect Transistor (FinFET). The analysis is done for fin lengths varying from 3nm to 12nm with and without source, drain contacts present at the bottom fin and compared with the Conventional Junctionless FinFET structure. The Novel Top Bottom Gated Junctionless FinFET with 3nm Lower Fin length and contacts on bottom fin shows 197 times improvement in switching ratio as compared to the Conventional Junctionless FinFET at the same gate length. The results reveal that the device shows enhancement in terms of switching ratio and allows better gate controllability when stacked against the Conventional Junctionless FinFET for various fin lengths.

Keywords*: Top Bottom Gated; FinFET; Fin Dimension Modulation; Switching Ratio; Junctionless*

Asymmetric Gate Stack Triple Metal Gate All Around MOSFET (AGSTM) for Improved Analog Applications

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Abstract: In this paper we have proposed and analysed Asymmetric gate stack triple metal gate all around FET (AGSTM) for improvement in performance for applications in the analog domain using SILVACO ATLAS 3D device simulation software. Previously junction less devices with triple metal have been discussed for the first we have proposed and analysed a Schottky barrier device of this nature apart from this we have done a comparative analysis of our proposed device AGSTM with other gate all around devices such as Single Metal Gate All Around (SMGAA), Triple Metal Gate All Around (TMGAA), Gate Stack Single Metal (GSSM), Gate Stack Triple Metal (GSTM) and Asymmetric Gate Stack Single Metal (AGSTM) to check its suitability for its use in analog applications. The proposed device gives excellent performance in terms of drain current, transconductance, output conductance, current gain, maximum transducer power gain so it is extremely suitable for analog applications.

Keywords: *Asymmetric Gate Stack; Triple metal; Short Channel Effects (SCEs); Hafnium Oxide (HfO2)*

Multiband Resonance in Symmetry Broken Planar Terahertz Metamaterial

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Abstract: This manuscript presents the experimental demonstration of multi-band Fano resonances in planar terahertz metamaterial. The proposed metamaterial structure resonates at two distinct frequencies at 0.25THz and 0.4275THz respectively. The broken in the structural symmetry provides two other Fano resonances at 0.27 and 0.31THz respectively in addition to the desired resonances. The variation in the two Fano resonances for broken geometrics is studied numerically using CST Microwave studio software and the geometrical parameters are optimized for the desired resonances. The transmission characteristics for various incident angles have been done to analyze the structure for angular independency operation. In addition, the current distributions through the surface of the metamaterial structure are also studied numerically. The optimized metamaterial geometry can be fabricated easily using femtosecond laser micromachining process.

Keywords*: Metamaterial; Fano; Symmetry broken; Laser; terahertz; modulation; non-ionizing; imaging*

Analog Performance of Dual- Metal Gate Stack Architecture of Junctionless Accumulation-Mode Cylindrical Surrounding Gate (DMGSA-JAM-CSG) MOSFET

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Abstract: This paper analyses a refined edition of Junctionless Accumulation Mode (JAM) MOSFET, i.e., Dual- Metal Gate Stack Architecture of JAM Cylindrical Surrounding Gate (DMGSA- JAM- CSG) MOSFET. In this device, use of dual metal gates and a high-k gate stack is leading towards the enhancement of the device's performance. Simulation of this device has been accomplished and the results are also compared with JAM-CSG MOSFET. It is seen that this device possesses improved characteristics, i.e., increased drain current, higher transconductance, lower output conductance, improved intrinsic gain and early voltage, high I_{on}/I_{off} ratio and reduced subthreshold slope. Thus, the overall performance of the device is much better and therefore is more capable for high gain amplifier and high speed switching applications. The simulation has been conducted on ATLAS 3-D device simulator.

Keywords*: Accumulation Mode MOSFETs; double gates; gate stack; junctionless transistor.*

Design of a Modified 8-bit Semiflash Analog to Digital Converter

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Abstract: A modified 8-bit semiflash Analog to Digital Converter (ADC) with reduced comparator count and having the same speed of a full flash ADC is reported in this paper. During the first half of the clock cycle, four bits from the MSB side are determined while in the latter half of the clock cycle, four bits from the LSB side are evaluated. Thus the designed circuit is as fast as a full flash ADC. For an 8 bit ADC, 4 bits from the MSB side remain unaltered for every sixteen successive bit combinations, starting from the first one, i.e., 0000 0000. Thus, 256 bit combinations can be divided into 16 different ones. The 4 bits from MSB and LSB sides are successively stored in an 8-bit latch. Thus the designed 8 bit ADC is realized in only one clock cycle employing 15 comparators, compared to 255 comparators for a full flash 8 bit ADC. The proposed ADC will require very small die area and power consumption will be low.

Keywords: *Bit segmentation scheme; Flash ADC; field, half flash; MFFADC; voltage estimator*

Impact of channel splitting on gate all around tunnel field effect transistor (gaatfet)

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Abstract: In this paper, we examine the concept of channel splitting in Gate All Around Tunnel Field Effect Transistor (GAATFET) and its impact on the performance of the device. The TFET device proposed in this work is designed for a channel length of 20nm and the channel region is divided with equal lengths on the same side. The doping concentration has been kept more towards the drain side channel. Numerical simulation using CAD device simulation software has been performed for investigating device performance. Results have been compared with the uniform channel GAATFET. Simulation results show that there is a reduction in off current by 1 decade in the case of split channel GAATFET. Further, a larger difference is found in the electron current density (ECD) of the split channel GAATFET. The subthreshold swing is also found to decrease to a value of 33.14 mV/decade. The threshold voltage was found to be 0.092V.

Keywords*: GAATFET, doping concentration, split channel, subthreshold swing, threshold voltage*

Simple and easy one step method for synthesizing ZnO nanorods for high frequency device application

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Abstract: ZnO nanorods were synthesized by thermal decomposition method calcined at two different temperatures 400℃ and 600℃ for three hours. Prepared ZnO nanorods were characterized with different characterization methods. Structural analysis was performed by X-ray diffraction (XRD) and found single phase formation with wurtzite hexagonal structure. Surface morphology was visualized by field emission scanning electron microscope (FESEM). FESEM images clearly showed formation of ZnO nanorods for both samples. The dielectric results showed that sample sintered at 600℃ is more suitable for high frequency memory device application due to its high dielectric constant 60 and low dielectric loss 0.9 at 1 KHz.

Keywords*: ZnO nanorods; thermal decomposition method; dielectric study; high frequency device application*

Solar Powered Home Automation System Enhanced with Internet of Things and Network Time Protocol Server

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Abstract: In the global scenario comfortable living conditions with domestic automation has become an essential part of our daily life. By making our house smart to lift up our comfort zone, we're also managing our necessity of water and electricity in a smart way to minimize wastage and reduce pollution level by using alternative source of energy. This paper presents the complete design of an IoT based solar power control system and water level control system for home automation. The required parameters are managed using the IoT device along with Network Time Protocol Server, which allows real time data sensing, processing and controlling in a smarter way. Blynk platform has been incorporated for remote measurement and control of required parameters.

Keywords*: Solar Power, Internet of Things, Home Automation, NodeMcu, Blynk.*

Symmetrical and Asymmetrical Fault Studies of Wind-Farm Embedded Power Network

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Abstract: In present electrical power system, there is a growing interest on study and analysis of AC grid connected wind power generation by research community throughout the world. In the same time there is always a concern for power system protection, and huge emphasis is given to studies based on various obstacles encountered by a power network under various fault conditions. In this context, this paper provides a thorough investigation of various types of faults occurring in a 225/90 kV power network, the operating frequency being 50 Hz., using simulations conducted in DIgSILENT PowerFactory Version 15 software. The concerned power system consists of two wind farms (one connected to the east side of the grid and the other connected to the west side). Symmetrical and asymmetrical fault conditions are simulated at various locations of the network. In the study, various responses of individual voltages and currents at both the bus bars and the generator side using many parameters are observed. In addition, various plots have been shown to minutely observe the effect of the fault with respect to time under varying operating conditions. This study will surely aid in providing variable insights regarding power system protection and modelling.

Keywords*: wind power; fault analysis; DIgSILENT; PowerFactory; power system protection*

Complementary Memresistive Switch Based Realization of Delay and Toggle Flip-Flop

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Abstract: *In-memory* computing architecture is gaining momentum to replace the classical Von Neumann architecture with high computational speed. Memristor is a suitable candidate to implement memory and logic in the same platform for performing in-memory computation for high execution speed and performance. This work addresses flip-flop designs using Complementary Memristive switch (CRS) which shows better results in comparison with the earlier designs implemented using different memristive logic styles. The proposed flip-flops are simulated using SPICE which utilizes less number of execution steps with lower count of memristive elements. The power consumption in proposed Delay flip-flop and Toggle flip-flop using CRS reduced by 46.8% and 51.53% as compared to the MAGIC In-memory design which uses pure memristive elements.

Keywords*: Memristors; Complementary Memristive Switch; Flip Flop.*

Serial and Parallel based Intrusion Detection System using Machine Learning

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Abstract: Cyber attacks have been the major concern with the growing advancement in technology. Complex security models have been developed to combat these attacks, yet none exhibit a full-proof performance. Recently, several machine learning (ML) methods have gained significant popularity in offering effective and efficient intrusion detection schemes which assist in proactive detection of multiple network intrusions, such as Denial of Service (DoS), Probe, Remote to User (R2L), User to Root attack (U2R). Multiple research works have been surveyed based on adopted ML methods (either signature-based or anomaly detection) and some of the useful observations, performance analysis and comparative study are highlighted in this paper. Among the different ML algorithms in survey, PSO-SVM algorithm has shown maximum accuracy. Using RBF-based classifier and C-means clustering algorithm, a new model i.e., combination of serial and parallel IDS is proposed in this paper. The detection rate to detect known and unknown intrusion is 99.5% and false positive rate is 1.3%. In PIDS (known intrusion classifier), the detection rate for DOS, probe, U2R and R2L is 99.7%, 98.8%, 99.4% and 98.5% and the False positive rate is 0.6%, 0.2%, 3% and 2.8% respectively. In SIDS (unknown intrusion classifier), the rate of intrusion detection is 99.1% and false positive rate is 1.62%. This proposed model has accuracy similar to PSO – SVM and is better than all other models. Finally the future research directions relevant to this domain and contributions have been discussed.

Keywords*: machine learning; intrusion detection schemes; DOS; Probe; R2L; U2R; PSO-SVM; RBF; C-mean clustering*

L-shaped piezoelectric energy harvester for low frequency application

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Abstract: In this paper, the L-shaped piezoelectric (PZ) cantilever structure has been designed, which is suitable for low frequency application. The size of the designed structure is within 5 mm. This makes it suitable to power any wireless sensor nodes for machine monitoring system. The L-shaped cantilever structure helps in reducing resonant frequency. It is able to achieve resonant frequency of 79.5 Hz. The proposed structure is simulated at 1g excitation acceleration and generates the output voltage of 11.6 V at its natural frequency. The proposed L-shaped PZEH generates an output power of 10.8 μW at its resonant frequency.

Keywords*: Piezoelectric, Energy Harvester, L-shaped, Stress, Resonant Frequency*

Study on Power Quality Phenomena of Grid connected AC Micro-grid

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Abstract: In recent electrical power system, there is a greatest interest on operation, control and performance of AC micro-grid by research community throughout the world. In this context, this paper investigates power quality issues of grid-connected AC micro-grid. The micro-grid consists of two wind farms (one is fixed speed type and other is variable speed type), a solar power plant and a mini hydel plant at point of common coupling (PCC). The grid is modeled as AC voltage source in series with impedance. The voltage and frequency at PCC are 600V and 50 Hz respectively. All heterogeneous non-conventional energy sources are interfaced to the main grid through different types of power electronics converter(s) and a common transformer. In the study, PSCAD software is used to model the grid-connected AC micro-grid. Various responses of individual entities and at grid-side variables are observed. Here, various power quality problems have been monitored from the model of AC micro-grid under dynamic operating conditions like switching of non-linear load and power factor improving capacitor. This study will be helpful to develop strategy in future for mitigating or suppressing power quality problems in the AC micro-grid.

Keywords*: AC micro-grid; wind power; solar power; hydel power; power quality; PSCAD*

Strained SiGe Channel TFTs For Flexible Electronics Applications

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Abstract: For More-than-Moore (MtM) applications, the design and development of a strain-engineered flexible SiGe channel thin-film transistor (TFT) are reported for the first time. We demonstrate a simple and viable approach to realize strained-SiGe channel RF transistors on flexible plastic substrates using 3D technology CAD (TCAD) simulations. The device has great potential in low-power and high-speed flexible or stretchable electronics applications.

Keywords*: TFTs; SiGe; Flexible Electronics*

Parametric analysis for varied gate work function in trigate n-channel finfet

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Abstract: In this paper, a 3D Trigate FinFET is implemented and simulated with the help of Silvaco TCAD. The electrical characteristics such as I_{on}, I_{off}, the ratio of on to off current, threshold voltage and subthreshold swing are compared by varying the work function of the gate metal of the device. The results show that although the threshold voltage escalates on raising the work function of the gate but it also decreases the leakage current thereby improving the on to off current ratio. So the short channel effects of the n-channel Trigate FinFET devices can be optimized by controlling and adjusting the gate work function.

Keywords*: TG SOI FinFETs; Work function; Silvaco TCAD; threshold voltage; leakage current*

Linearity Investigation of Ultra-Low-Power Cylindrical SOI Schottky Barrier MOSFET for Biomedical and 5G/LTE Circuits Application

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Abstract: Non-linearity is a major challenge for 5G/LTE communication circuit designers. Also, OFF state power consumption in circuits used for biomedical body implant circuits is also a major challenge. Linearity and OFF state power consumption analysis are performed for cylindrical SOI schottky barrier(SB) MOSFET, by extracting FOM's like gm_2, gm_3, VIP_2, VIP_3, IIP_3, IMD_3, 1-$dB_{CP,}$ and I_{OFF} current. The results are compared with dielectric pocket (DP) SB MOSFET and schottky barrier MOSFET.

Keywords: *Non-linearity, harmonics, I_{OFF} current, OFF state power.*

Generalized Memristor Model using Simulink and its Rectification for Sinusoidal and other Periodic Signals

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Abstract: This paper introduces a method to reset the Memristive Devices for high-frequency operation under periodic excitation. It builds upon the existing Generalized Memristor Model and seeks to develop a Simulink/Simscape-based Model, incorporating the proposed approach to analyze the behaviour
of the Memristive Devices.

Keywords*: Memristors, Model, Reset-Voltage, Simulink, Simscape*

Gate - Stack Dual Metal (DM) Nanowire FET with Enhanced Analog Performance for High Frequency Applications

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Abstract: A Gate-Stack dual metal nanowire field effect transistor (4H- Silicon Carbide) is analyzed using ATLAS 3-D device simulator to enhance the analog performance of semiconductor devices for high frequency applications. Gate- Stack dual metal nanowire field effect transistor (4H-SiC) results have been compared with Nanowire field effect transistor, Nanowire field effect transistor having (Silicon Carbide Substrate) and dual metal nanowire field effect transistor (Silicon Carbide) substrate. This is done by introducing a Gate-Stack having high k-dielectric material, Hafnium oxide (HfO_2) along with Aluminum oxide (Al_2O_3) gate dielectric.It exhibits higher drain current I_{ds}, Transconductance ($g_{m)}$, output conductance ($g_{d)}$ and cut off frequency ($f_{T)}$. The subthreshold slope obtained for gate –stack dual metal nanowire field effect transistor (4H-SiC) is 63.96 (mV/decade) which is closest to the ideal value as compared to other analogous nanowire field effect transistor which makes it extremely superior for high frequency applications.

Keywords: *Dual metal; Gate- stack; 4H-SiC; Frequency; Sub threshold; transconductance; SCE*

An Area Efficient VLSI Architecture for 1-D and 2-D Discrete Wavelet Transform (DWT) and Inverse Discrete Wavelet Transform (IDWT)

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Abstract: Several discrete wavelet transform architectures have already been introduced due to their wide range of applications in the field of image, video and speech signal processing. In this paper, an area efficient VLSI architecture for 2-dimensional discrete wavelet transform (DWT) and inverse discrete wavelet transform (IDWT) have been proposed. Theoretically, the hardware and timing analysis of existing and proposed architectures are presented. The proposed and several existing architectures are also simulated and synthesized for virtex-4 FPGA device. Performances of all architectures are observed in terms of slice, slice flip-flops, clock frequency using Xilinx ISE Design Suite 14.7 Synthesis tool. Also the numbers of slice LUTs, slice registers, clock frequency, and delay of proposed DWT and IDWT architectures are found using virtex-7 FPGA device family.

Keywords*: Discrete Wavelet Transform (DWT); Inverse Discrete Wavelet Transform (IDWT); Daubechis-4 Wavelet; Field Programmable Gate Array (FPGA); Very Large Scale Integration (VLSI)*

Efficient rectifier for piezoelectric energy harvester using active diode

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Abstract: Ambient energy harvesting using piezoelectric material needs a rectifier for ac to dc conversion. Piezoelectric energy harvester (PZEH) generates very low-level output and therefore, the rectification efficiency of the rectifier needs to be high. The voltage drop across the rectifier components which commonly use diode connected MOSFETs, is a major source of power loss. To reduce the voltage drop, in this paper we propose use of active diode as the rectifier component of the bridge rectifier circuit used for PZEH. The active diode minimizes the forward voltage drop to 21 mV. The proposed bridge rectifier circuit can extract maximum 91 % of the power provided by the piezoelectric energy harvesting device. The use of active diode in the bridge circuit improves the power conversion efficiency by 49 % to that of the diode connected MOS based BR.

Keywords*: Piezoelectric energy harvester; Full Bridge Rectifier; forward voltage Drop; Conversion efficiency*

All-Optical Frequency Encoded Dibit-based Half Adder using Reflective Semiconductor Optical Amplifier with Simulative Verification

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Abstract: In the modern era, high-speed signal communication and computation increase optical reliability. Therefore, optics is a powerful candidate for implementation in different logic gates, combinational circuits, devices, optical computers, etc. The design of all-optical frequency encoded dibit-based half adder is devised in this communication. Some papers focus on the advantage of the precision of dibit logic by carrying out logic operations on dibit representation technique. This devised dibit-based design operates with a high speed as well as it reduces the bit error problem by increasing the high signal-to-noise ratio. Frequency encoding is the most reliable encoding technique because of its unaltered nature in reflection, refraction, absorption when propagates in long-range. In this devised design reflected semiconductor optical amplifier is used to fulfill the purpose of optical switches. The operation of the devised design is verified through proper simulation using MATLAB Simulink (R2018a) software.

Keywords*: Optical Communication; Dibit-based logic system; Frequency encoding; Reflective semiconductor optical amplifier; adder*

Numerical Simulation of GaN-BTG MOSFET for Suppression of SCEs

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Abstract: The detailed study of GaN-BTG MOSFET where GaN is used as a substrate in lieu of silicon and at the gate terminal, a stacking of silicon dioxide (SiO_2) and hafnium dioxide (HfO_2) is placed in a conventional trenched gate structure to obtain the proposed device. This paper addresses the comparative study of electrical characteristics such as transfer characteristics, output characteristics, transconductance, higher-order transconductance, transconductance generation factor, output conductance has been obtained for the proposed device by performing simulation using TCAD. The results validate the superiority of the proposed device in terms of performance.

Keywords: *GaN-BTG MOSFET; Conventional trenched gate MOSFET; Short Channel Effects; Higher-order transconductance; Transconductance generation Factor*

Features of Snapback in Compact Memory Devices for High Performance Integrated Circuits

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Abstract: This paper provides physical insight of ZRAM (Zero Capacitor RAM) based on space charge limited (SCL) model. 2-D NMOS device is characterized and its operation area is explored by technology computer aided design (TCAD). In particular, with proper selection of the current ramp at the drain, carrier electrostatics is examined. It analyses the snapback phenomenon in capacitor-less memory under high current application at drain of gate grounded NMOS devices. Physics of current crowding phenomenon under ambipolar injection from the drain is analyzed. The work evaluates the electrostatics of the problem in terms of surface and bulk to understand mechanisms of current flow. An analytical model is established to show lesser impact of surface bipolar turn-on under snapback and its larger impact in the bulk impacted by applying bias to the gate.

Keywords: Snapback*; High Current; Breakdown, ZRAM, Ambipolar Current, GGNMOS*

Minimizing Wirelength with Bend Reduction using Gradient Descent PSO Hybrid in VLSI Global Routing

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Abstract: Contemporary evolution in assembling billions of transistors in a solitary bite of VLSI chip and additionally the decrease in the dimension of chip from micrometer to nanometer level demonstrates increased complexity where VLSI global routing play the crucial role in reducing delay and power loss. The objective of minimizing overall wirelength of interconnected nodes formulated as Rectilinear Steiner Minimal Tree (RSMT), a NP-complete problem and subsequent bend reduction increases the possibility of via minimization in the later stage of VLSI physical design thereby achieving less power loss and less interconnect delay. Notable computational approaches had been tried out by researchers but finds limitation for higher dimensional layout. In lieu of overcoming increased complexity metaheuristic algorithms like basic Particle Swarm Optimization (PSO), Genetic Algorithm (GA), Ant Colony Optimization (ACO) and their hybrids have already found their fruitful application for this purpose but sometimes with the limitation of divergence. This paper proposed a hybrid of Gradient Descent algorithm along with Particle Swarm Optimization (PSO) thus yielding an evolutionary hybridized optimization approach (GDPSO) which is implemented for discovering the RSMT followed by reducing the bend quantity. Moreover the proposed algorithm is compared and analyzed with the existing metaheuristic approach and Geosteiner benchmark to establish its more effectiveness in VLSI routing paradigm.

Keywords: *VLSI Global Routing, Bend Reduction, RSMT, PSO, Gradient Descent.*

Technology Computer Aided Design of a Novel Fully Gate Covered Channel Junctionless SOI FinFET for high performance analog applications

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Abstract: This work presents the analysis of various analog performance parameters of a fully gate-covered channel junctionless (JL) SOI FinFET with a high-k dielectric gate oxide, which is compared to the conventional junctionless SOI. The device exhibits an increase in the performance characteristics with respect to the conventional device, in terms of the switching ratio (about 100 times), transconductance (by about 10 times) and parameters like early voltage and intrinsic gain also improved. The devices also show a great reduction of DIBL, by about 60 mV/V and better SCE characteristics. These performance enhancements make the device suitable for certain applications involving high switching speeds and make them a good option for high-performance analog applications.

Keywords*: Junctionless (JL) transistor; fully gate-covered JL FinFET; analog performance; high-k dielectric*

A Simulation Study of 2-D Electron Gas in GaN HEMT for High- Speed Applications

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Abstract: The high-power GaN High Electron Mobility Transistors (HEMT) are used for next-generation high-speed R.F. applications. This work intends to simulate and analyze the $Al_xGa_{1-x}N$/GaN HEMT to obtain two-dimensional electron gas (2DEG). The variation of 2DEG concentration by varying the Al concentrations and width of the $Al_xGa_{1-x}N$ layer has been explored. This exhibits the importance of a polarization-induced inbuilt electric field. Our results confirm that the inbuilt electric field facilitates the high 2DEG density in nitride systems due to the transfer of carriers from the surface states, and it can be utilized to calculate the subband electron mobility of GaN HEMT structures.

Keywords*: 2DEG, GaN, AlGaN, HEMTs, polarization*

Investigation of III-V Tunnel FETs for Analog Circuit Design

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Abstract: A comparative analysis of TFETs and FinFETs analog circuits at technology node 20 nm and 16 nm is presented in this paper. For this purpose, we used the TFETs look-up table based Verilog-A model at 20 nm node and FinFETs PTM at 16 nm node having the same gate length of 20 nm as of TFETs. Comparison is done for resistive load common source amplifier and resistive load differential amplifier. For resistive load common source amplifier comparison at same g_m/I_d and same aspect ratio and for differential amplifier, it is at same aspect ratio and same supply voltage. Analog parameters such as gain, unity gain-bandwidth (F_T), and 3db-bandwidth are obtained from simulations and it clearly shows that TFETs are better in the analog application for sub-threshold voltage and higher voltage FinFETs have shown some improvement and are comparable to III-V hetero-junction TFETs and better than homo-junction TFETs.

Keywords*: Predictive technology model (PTM); tunneling field effect transistors (TFETs); low-voltage application*

Analysis of Dual Metal Gate Engineered SiGe/Si TFET based Biosensor: A Dielectric Modulation Approach

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Abstract: In this article, a highly sensitive and efficient label free biosensor based on dielectric modulation has been evaluated by considering the extended gate engineering mechanism along with the SiGe/Si heterostructure (H) tunnel (T) FET architecture. Moreover, the 2D simulations have been executed using SILVACO ATLAS TCAD tool. Besides, the proposed HTFET provides stability to the immobilized biomolecules within the sensing cavity because of the extended gate at the source/channel interface. The proposed SiGe/Si HTFET device shows impressive performance in terms of sensitivity against the variation of different neutral, positively and negatively charged biomolecules. Our results depict that the proposed device is capable of providing an ON Current Sensitivity (S_{ION}) of 7.5 x 10^9 for k = 12. Therefore, the DM-GE-HTFET (Dual Metal Gate Engineered HTFET) can be used as an alternative to the conventional TFET based biosensors.

Keywords*: Dual Metal, Gate Engineering, Heterostructure Tunnel FET, Dielectric Modulation, Sensitivity*

FPGA Implementation of an Image Watermarking Scheme based on Intensity Level Matching

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Abstract: The aim of this work is to develop FPGA architecture of such an image watermarking scheme that can overcome the tradeoffs among the major three qualities – imperceptibility, robustness, and payload. This proposed scheme, developed in spatial domain, can be performed to embed gray-scale watermark image into any single color-plane of a cover object. Embedding has been performed in such a manner that the watermark pixels of any particular shade can be inserted into cover image pixels having the same or contiguous shades. This way, the visual transparency of the embedded information has been improved. Efficiency of this proposed scheme has been assessed through some image quality metrics, and compared to the same of some new age image watermarking techniques. The comprehensive analysis asserts that this watermarking system is able to meet its goal successfully.

Keywords*: Watermarking; spatial; FPGA; robust; imperceptible*

In memory Computing based Boolen and logical Circuit Design using 8T SRAM

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Abstract: Digital logic and SRAM are important things in a computing system we all know that the number of transistors in a dense integrated circuit (IC) doubles about every two years that means the size of the transistor is decreasing but architecture which we are using was unchanged .for every computing system we expect the high performance and energy efficiency The power and productive shortcoming of von-Neumann gadgets has been featured lately because of the current spotlight on information concentrated applications, for example, man-made consciousness and AI. the primary moto behind the of the in-memory computing is to expand the throughput and productivity

Keywords*: von- Neumann architecture. In-memory computing, SRAM*

Impact of Au and Ag on the electrical parameters of MnO_2 Nanowires grown by Glancing Angle Deposition technique

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Abstract: The study of the effect of gold (Au) and silver (Ag) on MnO_2 nanowires (NW) were carried out by analyzing their impact on the parameters of the electrical characteristics. Firstly MnO_2 NW of length 250nm was fabricated on p-Si substrate using Glancing angle deposition (GLAD) technique. Secondly, Gold (Au) and Silver (Ag) contacts are then deposited on top of the NW. Extraction of the junction parameters like ideality factor; schottky barrier height, series resistance and interface index were carried out. Comparing the parameters of Au/MnO_2 NW and Ag/MnO_2 NW, Gold (Au) contact shows better performance as compared to Silver (Ag).

Keywords*: MnO_2 Nanowires; GLAD; Electrical characteristics; ideality factor; series resistance.*

Design and Analysis of III-V Tunnel FET based Energy Efficient Digital Circuits

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Abstract: The objective of this work is to incorporate a Lookup table based analytical model of TFET using Verilog-A in Cadence Design framework and thus using this integrated model we are able to design and simulate some of the digital circuits. The Look-up-tables are obtained from TCAD simulations. III-V materials are taken into consideration, as these devices are having higher driving capability as per ITRS Norms. A library is created in Cadence and based on N-type TFET P-type TFET, Inverter, NAND, NOR, half adder are realized. A comparative analysis is made with the state of arts of FinFET using 22nm technology. We proposed an Inverter circuit using hybrid TFET-FinFET. As the TFET technology can attain a low subthreshold slope of nearly 40mV/decade, we opted for this technology for designing. Therefore, this promotes the TFET-based circuits to work with a 0.5V supply voltage which leads to a reduction in dynamic power consumption and leakage current when compared to the current CMOS technology. As the results suggest that many more advantages and we can choose TFET for designing. The schematics and circuit simulation is done using the Cadence Virtuoso tool.

Keywords*: Homojunction TFET; FinFET; Hybrid TFET-FinFET;*

Design and Performance Analysis of Z-Shaped Charge Plasma TFET-based label-free Biosensor

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Abstract: Performance analysis of a doping-less Z-shaped charge plasma tunnel field effect transistor-based (CP-TFET) label-free biosensor is done with misaligned cavity region on the source and channel. The biosensor device is designed using charge plasma technology. We use suitable metal work function to create source, channel, and drain regions. This device is used for label-free electrical identification of biomolecules such as, uricase (k=1.54), streptavidin (k=2.1), biotin (k=2.63), 3-aminopropyltriethoxysilane (APTES) (k=3.57), keratin (k=8), and gelatin (k=12). The results shows better sensitivity in terms of I_{ON}, I_{OFF}, sub-threshold swing (SS), I_{ON}/I_{OFF} ratio as compared to FET-based biosensors. All simulations have been performed in the Silvaco ATLAS 2D device simulator.

Keywords*: charge plasma, biomolecule, biosensor, TFET.*

Neural network based soft sensor for critical parameter estimation of gas turbine engine

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Abstract: It is often difficult to implement a instrumentation in the intricate passages of a Developmental Aero Gas Turbine Engine(GTE). These instrumentation are to be critically monitored and evaluated for estimating the performance and health of the GTE during the testing before the development attains maturity into a qualified flying machine. Soft sensors are often implemented to infer parameters which are otherwise hard to measure variables. In this work a ANN based soft sensor approach is developed for estimating a set of five parameters which are hard to measure temperatures and pressures of secondary air system (SAS) of a GTE. The soft sensor is developed using a large sample set of 50000 readings collected over a period of time during the developmental testing of a GTE program. ANN model is developed with multiple inputs and output nodes. Optimum numbers of hidden layers are chosen. Using the main measured gas path pressures , temperatures and spool speeds as the input, the soft sensor predicts the various SAS parameters which can be used for both online monitoring and off line data analysis.

Keywords*: Soft sensor ;Gas turbine engine; Neural network*

Simulation of Low Power DVCC Based LNA for Wireless Receiver

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Abstract: In this research paper, a new configuration realizing LNA using CMOS differential voltage current conveyor (DVCC) based on low power, free from trans-conductance variation using Low-voltage PMOS bulk-driven cascade current mirror (P MOS BDCCM) is proposed. The circuit uses four DVCCs as active elements and together with two capacitors and five resistors as passive elements, only one current mirror. The use of this active component makes the implementation simple and attractive. The functionality of the circuit is tested using Tanner simulator version 15 for a 70nm CMOS process model also the transfer function realization is done on MATLAB R2017a version, and various simulation results are obtained. Simulation results are included to demonstrate the results.

Keywords*: Low Noise Amplifier; Transconductance; Bulk-driven cascade current mirror; Differential Voltage Current Conveyor (DVCC).*

Exploration of 9T SRAM Cell for In Memory Computing Application

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Abstract: Von-Neumann Architecture is the pillar of the current memory computing system & this architecture has an issue of power wall and memory wall. These walls have a big importance on computing in current time because of high eminence on data insensitive application. For this wall In-Memory Computing (IMC) is a good architecture to overcome with this issue. In this paper we are implementing In-memory computing based Boolean circuit with help of 9T SRAM and latch type sense amplifier. The Boolean operations are implemented using Generic 250 nm technology and 5 Volt VDD. We are implementing NAND, NOR, AND & OR logical Boolean gates using IMC.

Keywords*: IMC (in memory computing), VNA (Von-Neumann Architecture), SRAM (static random-access memory)*

The Performance Analysis of 70nm T-gate InAlN/AlN MOS-HEMT using Graded Buffer

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Abstract: In this paper, we have proposed the 70nm T-gate InAlN/AlN MOS-HEMT with graded buffer. The gate oxide and graded buffer effect on DC and analog parameters are investigated and briefly compared with the standard GaN-HEMT structure. It has been observed that linearly grading the Al composition in the buffer layer significantly enhances the device's performance. Various analog FOMs such as transconductance (g_m), output conductance (g_d), transconductance generation factor (TGF), intrinsic gain (A_v), early voltage (V_{EA}) have been investigated using the Silvaco-Atlas simulator. Simulated results confirmed that grading the buffer layer and using the high k-gate dielectric significantly enhance the switching ratio (10^{14}), transconductance (900mS/mm), and improve all the analog FOMs, which confirmed the suitability of the proposed device for digital and analog applications**.**

Keywords*: Graded, heterostructure, T-gate, Analog.*

Stress-Engineered AlGaN/GaN High Electron Mobility Transistors Design

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Abstract: The performance of AlGaN/GaN High Electron Mobility Transistors (HEMTs) can be improved using the strain engineering technique. We have investigated the role of nitride passivation layer induced stress/strain on the spontaneous and piezoelectric polarization in nitride/AlGaN/GaN heterostructures with particular emphasis on the drain current. The variation of stress profile due to change in nitride layer thickness has been presented. The study encompasses topography simulation, which realistically reproduces an experimental HEMT and the stress distribution in the device.

Keywords: *Stress/strain engineering; GaN/AlGaN; HEMT; piezoelectric; spontaneous polarization*

Harmonic Suppression in a Folded Hairpin-Line Cross-Coupled Bandpass Filter by using Spur-Line

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Abstract: The design of a compact bandpass filter using cross-coupled half-wavelength open-loop microstrip hairpin resonators with improved stopband skirt characteristics and spurious harmonic suppression is presented in this article. The proposed filter has a fractional bandwidth of 5% subject to the design frequency of 2.5 GHz for WLAN applications. At first, a fourth-order compact hairpin-line bandpass filter has been designed by arranging the doubly folded hairpin-line cells symmetrically in a cross-coupled configuration. Accordingly, a size reduction of 11.36% over folded hairpin-line filter has been achieved with an improvement in the skirt characteristics by placing two deep transmission zeros at the edges of the passband. However, the benefits of cross-coupled configuration have been overshadowed by the presence of spurious harmonics with an attenuation level of 10 dB. Subsequently, spur-line has been employed in each coupled section of adjacent folded hairpin-line cells for achieving modal phase velocity compensation. As a result, an extended stopband with a rejection level of 35 dB up to $3.16f_0$ and overall size reduction of 20.46% has been achieved.

Keywords*: bandpass filter; cross-coupled; harmonic suppression; hairpin-line; wide stopband*

A Novel Junction Less Dual Gate Tunnel FET with SiGe Pocket for Low Power Applications

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Abstract: A novel junction-less dual gate tunnel FET device with P+ $Si_{1-x}Ge_x$ pocket near the source end is introduced in this paper. The device exhibits sharp subthreshold slope of 63.5mV/dec, very high I_{ON}/I_{OFF} ratio of 10^{11} and low drain induced barrier lowering (DIBL) of 22.2mV/V. The junction less behavior and high-k gate oxide/high work function gate contact, boosts the ON current in the device. The double gate enhances the control of the gate on channel conduction and improves the drain current. The P+ pocket near the source end having narrow band gap material $Si_{1-x}Ge_x$ drastically reduces the tunnelling length and increases the I_{ON}/I_{OFF} ratio. The device is designed and simulated on Visual TCAD (Cogenda) device simulator for 18nm gate length. The device is simulated for various pocket materials and gate contact/oxide combinations to propose the present one. It has been tested for various gate length and SiGe mole fraction variations. It is also found to be efficiently operational over a wide range of temperature from 200K to 400K.

Keywords*: Junction-less Double-gate tunnel FET; subthreshold slope; high-k*

A Dielectric Modulated MOS transistor for Biosensing

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Abstract: The study on biosensors is recent ubiquitous research in biomedical diagnosis and employed in wide range of applications as detection of disease-causing biomolecules, point-of-care monitoring of treatment, marker indicator testing, environmental monitoring, drug discovery, forensics and biomedical research etc. The biosensor devices convert biomolecule recognized events to detectable signals. A wide range of techniques can be used for the development of biosensors. This paper initially provides the investigation for biosensing of biomolecules by analyzing and summarizing remarkable studies on heterostructure MOS devices which can capture biomolecules in the designated device regions. A dual-gate MOS device having cavity regions which can trap the biomolecules has been proposed and simulated to study electrical characteristics and threshold variation. The device can sense and detect the presence of biomolecules of dimensions up to 500nmx60nm. The proposed device can be further calibrated for several device and design parameters. Accordingly, the simulated results would be analyzed to report trade-off and other significant features to develop noble heterostructure MOS devices for biosensing.

Keywords*: MOS; Biosensor; Dielectric; Biomolecule; Heterostructure.*

A Review on Machine Learning Approaches for Predicting the Effect of Device Parameters on Performance of Nanoscale MOSFETs

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Abstract: This review investigates the possibility of using Machine Learning as a replacement for numerical TCAD device simulation. As the chip design is getting complex to incorporate more and more functionality in the devices, many chipmakers started exploring advanced techniques of machine learning to get rid of some big challenges faced by IC industry. In Machine learning, advanced algorithms are utilized to identify patterns in data and to predict about the required information. Machine Learning finds its application in semiconductor fabrication as well as parameter extraction in device modeling. It is also used in prediction of device reliability and its analysis. This work proposes to utilize machine learning method to establish mapping between the performance parameters and structural parameters of the nanoscale MOSFETs. Methods using Machine Learning are fast, highly efficient and computing resource saving over traditional methods.

Keywords*: Machine Learning, Artificial Neural Network, TCAD simulation, nanoscale MOSFETs*

Study of Lead-Free Perovskite and Quantum Dots Core-Shell Infrared Photodetector Integrated with the Silicon Technology

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Abstract: An approach for optoelectronic infrared detection is demonstrated by combining conventional silicon technology, lead-free perovskite-type material, and quantum dots core-shell. It is shown that the device is sensitive to wavelengths in the infrared range of the electromagnetic spectrum up to 1055 nm. The detector is characterized by a high responsivity of 947 mA/W at 1055 nm. The detectivity and the external quantum efficiency at the same wavelength are found to be 5×10^7 Jones and 114 % respectively. This is considered as very good performance and can be ascribed to the presence of a photoelectric effect, producing a voltage that affects the silicon/IR material interface, controlling the depletion layer. These results are a good initial step to further optimization of the lead-free perovskite-based optoelectronics realized with compatible silicon technology.

Keywords: *Infrared detection; lead-free perovskite; quantum dots core-shell; silicon technology*

A 0.6 V 1.6 nA Constant Current Reference with Improved Power Supply Sensitivity

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Abstract: This paper presents a low power current reference with improved power supply sensitivity. The proposed circuit is designed in SCL 180 nm CMOS technology and simulated using Cadence Virtuoso. It generates a reference current (Iref) of 1.6 nA at 0.6 V supply voltage (Vdd) at room temperature (27° C) with a total power consumption of 10 nW (0.6 V). A new circuit configuration based on composite transistor operating in weak inversion has been proposed in this work. The proposed circuit is an improvisation on beta-multiplier circuits proposed earlier. The circuit improves the power supply sensitivity of the current source and provides a better performance in terms of process variability.

Keywords: *low power, weak-inversion region, composite transistor, power supply sensitivity*

Variation of Rain Rate Effects for Terrestrial Communication at Frequencies above 10 GHz

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Abstract: The variation of rain effects for terrestrial communication are examined at frequencies above 10 GHz in the present study. Propagation parameters like attenuation coefficient and phase-delay coefficient are assessed for the rain filled medium. It is examined how the pulse is distorted while passing through rain cell. Specific attenuation is computed at different frequencies from 10 to 70 GHz and rain rate from 5 to 245 mm/hr for horizontal and vertical polarization. The effects of rain rate, the operating frequency and the propagation path length on the rain attenuation are tested. The impact of polarization type on terrestrial rain attenuation is examined here.

Keywords*: Pulse propagation, Rain attenuation, Rain rate, Terrestrial link*

A 2.24 NEF Current-Balancing Instrumentation Amplifier Using Inverter-Based Transimpedance Stage for ECG Signal Acquisition in 180nm Technology

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Abstract: A 2.24 NEF current-balancing instrumentation amplifier (CBIA) in 180nm technology was presented in this paper for wearable ECG monitoring systems. The proposed CBIA has two stages: a transconductance stage and a single-output-ended inverter-based transimpedance stage. The proposed system was able to achieve a low-noise and low-power instrumentation amplifier (IA) which are desirable for wearable health monitoring systems. The proposed system was able to meet the required standards for ECG recording systems published by ANSI-AAMI to be able to amplify the relatively weak ECG signal amplitude.

Keywords*: current-balancing instrumentation amplifier; transimpedance stage; transconductance stage; inverter-based;*

Radiation-Hardened Low Read Delay 12T-SRAM Cell for Space Applications

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Abstract: This paper proposes a Radiation-Hardened Low Read Delay improved 12-Transistor (RHLRD-12T) SRAM cell. By circuit optimization technique in 16-nm CMOS technology, the simulation results show that the proposed circuit can recover from single-event upset (SEU). It can also recover from single-event–multiple-node upset (SEMNU) that is induced due to the charge sharing among OFF-transistors. The proposed RHLRD-12T SRAM cell exhibits 1.34× (1.03×) longer (shorter) Write Access Time compared to RHBD-12T (RHBD-10T). It shows 1.2× (1.13×) improvement in Read Access Time compared to RHBD-12T (RHBD-10T). It exhibits 1.06× (1.32×) higher (lower) CWLM compared to RHBD-10T (RHBD-12T) SRAM cell.

Keywords: *Radiation-hardened SRAM cell 1; single-event upset (SEU) 2; single-event–multiple-node upsets (SEMNUs) 3.*

Effect of Drain Engineering on DC and RF Characteristics in Ge-source SD-ZHP-TFET

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Abstract: In this paper, a Ge-source is employed in split drain Z-shaped line TFET structure (SD-ZHP-TFET) and named as Ge-source SD-ZHP-TFET. The presence of split drain increases the tunnel width at interface of channel–drain, which reduces the ambipolar current (I_{AMB}). Also, the horizontal pocket at source region and the Ge-source boost the ON current (I_{ON}) of the SD-ZHP-TFET. A comparative study in terms of transfer characteristic and current ratio (I_{ON}/I_{OFF} and I_{ON}/I_{AMB}) among ZHP, SD-ZHP, and Ge-source SD-ZHP TFETs are highlighted through TCAD simulator. Furthermore, the impact of drain doping concentration of region 1 (N_{du}) and region 2 (N_{dl}) on transfer characteristic, I_{OFF}, and I_{AMB} are studied in proposed TFET. The Ge-source SD-ZHP-TFET provides I_{ON}/I_{OFF} and I_{ON}/I_{AMB} in the order of 10^9 and 10^{11}, respectively. Finally, RF/analog parameters like transconductance (g_m) and cut off frequency (f_c) is evaluated for Ge-source SD-ZHP-TFET.

Keywords: *Ambipolar current; Ge-source; RF/analog; split drain; transfer characteristics.*

Performance Analysis of Full Adder Circuits Using Different Static CMOS Based Threshold Logic Gate

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Abstract: Here Full Adder circuits have been designed and simulated using Ganged CMOS, Beta driven threshold logic and Capacitive Output wired logic respectively. The simulation studies of the circuits have been carried out in 130nm, 90nm, 65nm technology nodes using TSPICE software. The minimization of time delay, consumed power and physical size of such circuits are the most essential requirements for the use in artificial neural network. To find out the suitable CMOS static circuit based threshold logic for Full Adder, the essential parameters of the three circuits are compared and Capacitive Output wired logic-based design reveals the best result for all the parameters.

Keywords*: Threshold Logic Gate (TLG), β driven, Capacitive Output Wired Logic (COWL), Full Adder, Ganged CMOS.*

Double Gate-Pocket-Junction-less Tunnel Field Effect Transistor

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Abstract: In this Literature, a device with the concept of double gate junction-less tunnel field-effect transistor with a pocket region has been proposed and implemented. This device is made up of a Silicon wafer which is Heavily doped with N-Type species, divided into three regions Source-Channel-Drain without forming any junctions in between each region. A double gate concept also introduced in this proposed device which gains high control over the channel region and also isolated double-sided Auxiliary Gate upon source region with different metal work function to achieve the behaviour of TFET. A Pocket region also included in this device designing which yield better results. After the simulation, the results are as such that for a high-k dielectric material (HfO_2) of 20nm gate length yields excellent electrical characteristics at room temperature with ON current (0.1 mA/um), OFF current ($2x10^{-15}$mA/um), high I_{on}/I_{off} ratio ($\sim10^{12}$), and Sub-Threshold Swing (SS) of 60mV/decade, DIBL with a near value of zero as simulated through Technology Computer-Aided Design (TCAD). Hence the performance of this device DG-P-JLTEFT proves that it's a promising candidate for switching applications.

Keywords*: JLTFET, DIBL, SS, B-T-B-T, Pocket region.*

An Intelligent Weather Prediction System Based on IOT

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Abstract: Drastically changes in climate conditions reflect an unpredictable behavior of weather which becomes a real problem in daily life. The conventional forecasting model reports some inaccurate forecasts due to noncompliance with the climatic dynamicity. This paper proposed an improved solution for weather monitoring using low-cost GPS-enabled IOT devices, connected with different sensors. The sensed information is stored in the server to predict the weather parameters such as temperature, humidity, air pressure, etc. of any defined application region of interest. Here, some soft computing tools like SVM, KNN, DNN, Ridge, Linear Regression, and ANN have been explored on these weather parameters and establishes a correlation between conditions in a prescribed geographical location for upcoming days.

Keywords: *IOT, ANN, DNN, SVM, KNN, Weather Forecasting.*

GaN-Based Two-Stage Colpitts Oscillator for Wireless Power Transfer

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Abstract: This work investigates the applicability of a two-stage Colpitts oscillator based on GaN high electron mobility transistors (HEMT) for wireless power transfer applications. An inductive load is used both as part of the resonance network in the oscillator and as a power transmitting coil. Simulations and experimental results using commercial GaN transistors are provided.

Keywords: *GaN HEMT; Wireless Power Transfer; Colpitts oscillator*

Authentication and secure communication by Haar Cascade Classifier, Eigen Face, LBP Histogram and variable irreducible polynomial in (2^8) finite field

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Abstract: One of the most common way of verification is 'Face Recognition' which can also be implemented for communication between machines and humans. In industries, corporate sectors, financial exchanges, face detection and expression recognition are used for the purpose of security and authentication. Another area of interest is the communication of information securely (in this case it is face image). In this paper, for face detection process Haar-classifiers is used which produces an accuracy of around 99.4% from still images and 98.6% for video recordings. Using two algorithms i.e. LBPH algorithm and Eigenfaces face recognition is done. The former produces a recognition accuracy of 99.4% for still images and 99.6% from video recordings and latter produces accuracies of 98.6% and 99.5% for the same have been obtained. The paper also proposes a more secure modified AES, whose modification done by 43 variable S - Box generation out of which 9 S - Box return correct Inverse S – Box with the help of variable irreducible polynomial in GF (2^8) finite field. Thus every time using the variable irreducible polynomial [GF (2^8)] a new S- Box and inverse S-Box is generated which makes it difficult for the intruders to crack modified AES.

Keywords*: face detection, LBP Histogram, Eigenfaces, biometrics,haar cascade classifier, irreducible polynomial, AES, S – Box*

Impact of temperature and different types of trap charges on noise behavior of Non-uniform Body with Dual Material Source TFET (NUTFET-DMS)

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Abstract: This paper presents the noise analysis of non-uniform body with dual material source TFET (NUTFET-DMS) in absence and presence of various types and distribution of trap charges. Different noise performance describing parameters such as drain current noise power spectral density (S_{id}) and gate voltage noise power spectral density (S_{vg}) are investigated incorporating diffusion, generation-recombination (G-R) and flicker noise components. It is observed that at room temperature the device has a peak value of S_{id} and S_{vg} of 2.88×10^{-21} A^2/Hz and 6.67×10^{-4} V^2/Hz, 3.95×10^{-21} A^2/Hz and 9.1×10^{-4} V^2/Hz, and 2.57×10^{-21} and 5.93×10^{-4} when there are no trap charges, donor and acceptor types of trap charges respectively. It can be portrayed that at low temperature range the device is more sensitive to Gaussian distribution of donor types of trap charges when compared to acceptor types of trap charges at high gate to source voltage (V_{gs}) however, the reverse is true for low V_{gs}. Finally, it is observed that the noise of the considered device is negligibly affected due to uniform distribution different types of trap charges at high temperatures.

Keywords*: noise power spectral density, trap charges, noise, temperature*

Analysis of Double-Gate Junctionless MOSFET for Energy Efficient Digital Application

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Abstract: In this work, the performance of a Double-Gate Junctionless MOSFET (DGJLT) is reported for low power digital applications. The model is based physically, considering both the inversion and accumulation operating conditions. The analysis demonstrates the transistor behavior in the sub-threshold regime. SILVACO ATLAS TCAD tool is used extensively to validate the results of the proposed circuits. DGJLT transistors are found to have overall better performance at low supply voltage significantly. Hence, DGJLT transistor-based Inverter has been adopted for the reference. Analytical models of power dissipation, delay and power delay product (PDP) of the Inverter are detailed. The intended study gives a better view and understanding of the applications of energy efficient digital logic of the device at low power.

Keywords*: Double-Gate Junctionless MOSFET; low power applications; DIBL; Sub-threshold Slope (SS); Inverter; PDP*

Hardware realization and testing of multistage OTA buffer amplifier for heavy resistive load

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Abstract: Experimental study of operational transconductance amplifier (OTA) buffer amplifier configurations capable of driving resistive load < 100 Ω is presented in this paper. The OTA buffer configurations are designed using 0.18 µm SCL technology library and fabricated in semiconductor lab (SCL), Chandigarh. The experimental results show a good agreement with the theoretical and simulation results. A gain tuning of 0.5 V/V to 5 V/V is achieved with R_L equal to 50 Ω, maximum output swing of 1 V_{pp} with a supply voltage of ±0.9 V.

Keywords*: buffer amplifier, OTA, resistive load, tunable gain, transconductance*

Design of Duty-Ratio and Phase-Shift Control Circuits for MPPT of SPV Source using ZV-ZCS PSFB Converters

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Abstract: This paper presents two separate control circuits for a soft-switching phase-shift full-bridge (PSFB) pulse-width modulated (PWM) dc-dc converter. The PSFB converter is operated with maximum power point tracking (MPPT) controller to extract maximum power from a solar photo voltaic (SPV) source, either by controlling the duty ratio or by varying the phase-shift angle of switching gate pulses. The MPPT controller is used in the feed forward voltage control loop of SPV source. Both the duty ratio and the phase-shift controllers have been tried with conventional PID controller and linear quadratic Gaussian (LQG) controller for performance comparison in MATLAB environment. Finally, experimental studies have been performed to verify the ability of the controllers to extract maximum power from the SPV source using the PSFB converter.

Keywords*: Duty-ratio control, Phase-shift control, MPPT, PSFB converter, soft-switching converter*

Power dissipation estimation in SWCNT based interconnects

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Abstract: In this work power dissipation in a SWCNT interconnect of intermediate length (400um to 1000um) is estimated. Spice simulation is done for two different transmission line models of interconnect viz. distributed and Pi. Effect on power dissipation with the insertion of repeaters is also studied and comparison is done by varying the number of repeaters i.e. 2, 4, 6 & 8 repeaters. All the simulations are performed with RLC parameters calculated at 32 nanometer technology node. This has been observed that the power dissipation increases with increase in number of repeaters. The dissipation also increases with increase in length of the interconnect.

Keywords*: SWCNT, Interconnect, Repeater, Power-dissipation, Mean free path*

Highly Linearized GaN HEMT Based Class E/F3 Power Amplifier

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Abstract: The study of a GaN based mixed mode Class E/F3 power amplifier is presented in this article. For large signal simulations, we used the Cree transistor's nonlinear device model CG2H40010F and simulation is done at Keysight's Advanced Design System (ADS) platform. The harmonic balance (HB) simulator is run to select the most appropriate impedances for efficiency and linearity of PA. The simulation results are used to describe and analyze a Class E/F3 GaN-HEMT PA with lumped components operating at 3 GHz. The output power Pout at 1 dB compression is 40.23 dBm with a gain greater than 10 dB, drain efficiency (DE) ranges from 70% to 86% according to simulation results.

Keywords: *Class-E/F3;* power amplifiers*; DE; GAN-HEMT; IMN; OMN.*

A 1.8V 5-bit Segmented Current Steering Digital-to-Analog Converter

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Abstract: This paper presents the current steering Digital-to-Analog Converter (DAC). A segmented architecture has been implemented in this paper. A DAC has been designed to convert 5-bit digital input code to its analog counterpart current. The segmentation is done in such a way that the three most significant bits use binary-weighted current sources and the two least significant bits use unary-weighted current sources. The two least significant bits are converted to thermometric code as 2^N-1 current sources of unary weight are used. A cascoded current reference circuit is designed to bias the arrays of the current mirror circuit. A thermometric encoder is designed to code the two least significant bits of digital input to thermometer code. The DAC architecture using different types of switches is simulated and optimized to obtain better results. The maximum Integral Non-Linearity (INL) is 0.1498 LSB and the maximum Differential Non-Linearity (DNL) is 0.1256 LSB.

Keywords: *Current steering DAC, thermometer encoder, INL, DNL*

A Framework for Post Disaster Management using Device to Device Communication with Controlled Mobility and Opportunistic Routing

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Abstract: The Device to Device (D2D) communication has the ability of communicating in proximity and the integration of D2D in LTE-Advanced has come up with the possibility of forming a network with hand-held devices even in the absence of cellular network infrastructure. In this work we propose a post disaster management framework employing multi-hop D2D communication to restore communication and maintain relief work in disaster hit zones where communication system has collapsed completely. Clustering along with a concept of cluster core for efficient data collection by Data Mule has also been proposed. The intermittent nature of such D2D based communication system might lead to frequent and lengthy disconnection resulting delay in message delivery or loss of message. Opportunistic routing principle with bundle protocol on top of multi-hop D2D communication has been explored to address the network delay issue.

Keywords*: D2D; multi-hop; routing; mobility; bundle protocol*

The impact of oxide layer width variation on the performance parameters of finFET

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Abstract: In this paper, the performance of FinFET has been examined by changing the fin width which affects the device performance. The fin width has been changed by keeping the device width fixed and varying the width of the oxide layer by electrical characterization and simulation. The device width is fixed at 50nm and the oxide layer width is varied from 10nm to 3nm. Here five different parameters such as drain current (I_D), transconductance (g_m), cutoff frequency (f_T), gain bandwidth product (GBW), and power (P) are computed to study the effect of oxide layer width of the device. It has been observed from the simulation that at lower oxide layer width I_D and g_m show maximum value, and at medium value of oxide layer width f_T and GBW give better performance. The power consumption of FinFET is lesser when the oxide layer width reduces.

Keywords*: Fin, GBW, cutoff frequency, power consumption*

Highly Efficient and Compact Silicon based Novel Michelson Interferometer Modulator

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Abstract: We present a novel common mirror high-speed silicon Michelson interferometer (CMMI) modulator with two 380 μm-long PN diode phase shifters. The general Michelson Interferometer (MI) optical structure is an enhanced Mach- Zehnder interferometer (MZI) with both arms incorporated with reflective mirrors. In the proposed design, these two reflective mirrors are replaced by a single mirror employed as closed waveguide feedback loop at the output of 2×2 splitter/combiner unit. The light in the CMMI travels back and forth along the phase shifting waveguides and therefore doubles the effective length of light-carrier interaction. The proposed CMMI modulator shows high efficiency having a low figure of merit VπLπ of .71 V.cm to 0.85 V•cm for under the bias of 0.5 V to −4 V for a reduced insertion loss of 3.5 dB footprint, device count and fabrication variability. At 10 Gbit/s bitrate, extinction ratio of 12.5 dB and BER< is achieved thereby providing a great potential in the future optical interconnects.

Keywords*: Silicon Photonics, Photonic Integrated Circuits, Optical Interconnects, Mach Zehnder Modulator.*

Performance Analysis of Single Operational Transresistance Amplifier Based Bandpass Filter and Bandreject Filter

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Abstract: The authors have presented an operational transresistance amplifier (OTRA) based realization of bandpass filter (BPF) and bandreject filter (BRF) along with their different performance analysis like temperature analysis, worst case analysis and noise analysis. All the proposed filters are realized with a single OTRA and few passive components. All the simulation works are performed in SPICE with 180 nm CMOS model of OTRA. The proposed circuit has also been experimentally verified with AD844AN IC. The simulation and experimental results matches very well, establishing the validity of the work.

Keywords*: OTRA; CMOS; SPICE; Bandpass filter, Bandreject filter*

Impact of Ge Grading Profile on the Performance Characteristics of SiGe Heterojunction Bipolar Transistors

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Abstract: The DC characteristics of the different Ge grading profiles of the SiGe Heterojunction Bipolar Transistor (HBT) named as Linear increasing (LI), Symmetrically Triangular (ST), Hybrid Trapezoidal (HT), and Conventional Trapezoidal (CT) having 20% Ge contents is observed. After validation with experimental results, the four HBTs are simulated in the TCAD tool. The hybrid trapezoidal profile based SiGe HBT has the best DC characteristics like the highest current gain (294), the highest early voltage (-110 V), the lowest offset voltage (109 µV), and the lowest breakdown voltage (1.75 V) is observed.

Keywords*: Device Simulation, SiGe HBT, Ge grading profile*

Parametric Study of Silicon-Based Tubular Tunnel FET for Biosensing Application

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Abstract: In this paper, a Silicon Nano tube TFET has been proposed to sense the biomolecules. The simulations are carried out using the TCAD 3D tool. A nanocavity is made in the proposed device, and its ambipolar characteristics are taken as the sensitivity parameter. Sensitivity parameters are found by considering the level of filling of the cavity. All the simulations are done in the subthreshold region and considered the charge as well as neutral biomolecules. The biosensor is based on the dielectric modulated FET. In this tubular biosensor one gate is taken as the detecting gate and another gate is taken as the controlling gate. It is found that the implementation of tubular tunnel FET and gate engineering improves the device characteristics in terms of TFET performance and make it suitable for the proposed biosensor.

Keywords—*Silicon Nano Tube FET, FET based Biosensors, Dielectric Modulated FET, charged biomolecules*

Study of SiGe-Si Source Stacked in Silicon Nano Tube Tunnel FET

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Abstract: In this paper, the authors have analyzed the effect of stacked source on the Silicon nano-tube Tunnel Field Effect Transistor (TFET). Here half of the source region is Silicon, and the rest of the region is Silicon-Germanium (SiGe). The mole fraction (x) of the Silicon-Germanium is taken as 0.25. For simulation of TFET Kane model has been employed. By incorporating the SiGe in the source, the drive capability is increased, and by decreasing the value of the mole fraction, the leakage current of the device is reduced.

Keywords: *High-K dielectric; Silicon Nano Tube FET; I_{ON}/I_{OFF} ratio; Microelectronics; Nanotechnology; VLSI.*

Metaheuristic algorithms-based approach for optimal design of improvised fully differential amplifier for biomedical applications

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Abstract: This paper deals with metaheuristic-based approach for optimal solution of improvised amplifier for low power application keeping in special focus on area minimization. It implements a new technique in the circuit design to optimize the amplifier intended for low power low voltage biomedical applications. The methodology establishes the optimum aspect ratios and the biasing currents of the transistors, with reference to the analytical model of the amplifier so as to consider its area as an objective function. Various high-performance meta-heuristic optimization algorithms have been employed to determine the best possible aspect ratios at low computational cost and reduced complexity. A proper evaluation of all these algorithms discloses that the whale optimization algorithm is apt amongst all of them. The optimized parameters are estimated for the optimum area at high convergence speed. These results are cross-verified in contradiction to the simulation results in Cadence SCL 180nm environment. The algorithm sets up the aspect ratios and the biasing parameters of the transistors. This automated method of fixing up the parameters could possibly minimize the computational complexity of the problem and offer an accurate design solution for the amplifiers. These types of circuits are vastly explored in the design of preamplifier circuits of the neural amplifier to treat neuro-diseases like epilepsy, Alzheimer's disease, and many more.

Keywords: *metaheuristic algorithms; optimization; fully differential amplifier; aspect ratio;, computational complexity*

Energy Efficient Decoder Circuit Using Source Biasing Technique in CNTFET Technology

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Abstract: VLSI technology is essential for chip fabrication, and 3 to 8 decoder circuits are used in electronic gadgets; consistency of design, small, fast, in this proposed circuit, 3 to 8 decoder is implemented using 20nm CNTFET technology. 3 to 8 decoders are the key segments in some real-time applications. For the most recent couple of years, the minuscule size of MOSFET, which is under many nanometers, made some operational issues, for example, expanded entryway oxide leakage, intensified intersection leakage, high sub-limit conduction. The proposed model is recreated utilizing Cadence virtuoso with 20nm CNTFET nodes.

Keywords*: Body Biasing; Decoder; CNTFET; Source Biasing*

Comparative Study on Analog & RF Parameter of InAlN/AlN/GaN Normally Off HEMTs With and Without AlGaN Back Barrier

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Abstract: In this work, we have made a relative assessment of lattice-matched $In_{0.17}Al_{0.83}N$/AlN/GaN normally off HEMT device with AlGaN back-barrier (BB) and without back-barrier by using device simulator. The utility of AlGaN BB on the said E-HEMT relaxes the channel, which reduces the short channel effects. It also reduces the total gate capacitance and simultaneously improves the cut- off frequency. The numerical modellings, are done by the 2Dimenssional TCAD by means of HD mobility and matched with the previously accepted experimental result. Different device parameters are analyzed and compared with BB and without BB with the help of the numerical modelling. AlGaN back-barrier has further benefits in device parameters with comparison to without back-barrier i.e. less total gate capacitance and higher cut-off frequency. These outcomes prove the utility of proposed BB in such E-Mode GaN HEMTs can be a substitute way out in support of high power along with high-frequency purposes.

Keywords*: InAlN/GaN HEMT, AlGaN BB, normally off, Total gate capacitance, Cut off frequency.*

An SOI *n-p-n* Double Gate TFET for Low Power Applications

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Abstract: This article proposes a tunnel field effect transistor (TFET) based on *n-p-n* silicon body with double gates, one each over the two *p-n* junctions. The *p*-type source region is elevated as compared to the two *n*-type drain regions in order to create sufficient length for gate placement to cover the junctions. Electrical parameters have been systematically investigated through calibrated TCAD (technology computer aided design) simulations with objectives to reduce the ambipolar currents, and increase the ratio of on and off currents. Gate-on-drain length is an important parameter to control ambipolarity in the device, similar to gate-drain underlap length in conventional TFETs. Sub-60 mV/dec subthreshold swings, and drain current usually in order of tens of μA/μm have been observed. Gate workfunction engineering further shows the tuning of threshold voltage, and other electrical parameters.

Keywords*: SOI TFET; double gate; n-p-n; TCAD; BTBT*

Design Approach for Parameter Estimators for One-parameter First-order Scalar Plant

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Abstract: The paper analysis based on MRAC strategies for controlling a first-order system with considering the cost criterion for utilizing the gradient method. Adaptive control includes adjusting the uncertainty parameters develop by using the suitable controller to control in reality that the parameters of the plant being controlled change thoroughly because of altering in natural provisions or in a while in the plant itself. Planned paper deal with the application of dummy reference adaptable control conspires and the plant execution. We consider the simplest adaptive law or parameter estimators which are obtained by using the SPM. Simulation for the proposed first-order plant model of a scalar plant is performed in MATLAB – Simulink for a different assessment of adaptation gain. Due to the alteration in adaptation gain, the adaptation mechanisms also altered and effects on results are evaluated. On the deviation of plant parameters to ensure global stability, we consider the Lyapunov stability approach for the proposed first-order closed-loop dynamics system.

Keywords*: Static Parametric Model (SPM); Model Reference Adaptive Controller (MRAC); Lyapunov method; Gradient method; Adaptation gain.*

Ultra Low-Power Low-Pass Filter Design for Wearable Biomedical Applications

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Abstract: Low-pass filter (LPF) is an important circuit block used in System on Chips (SoCs) for wearable biomedical applications. However, designing a LPF with low power consumption and negligible Process, Voltage and Temperature (PVT) dependency is a challenging task. We in this work report design of Complementary Source Follower (CSF)-C LPF which uses composite PMOS devices and Common Mode Bulk-feedback (CMBFB) for achieving ultra-low power operation. The proposed LPF circuit has been simulated in standard CMOS 0.18 µm process using BSIM3V3 models. The proposed LPF consume 0.064 nW power from 0.5 V voltage supply at supply current of 0.128 nA with dc gain of -3.6 dB, bandwidth of 200 Hz and Figure of Merit (FOM) of 0.004. The proposed LPF can be used in future low-voltage biomedical systems for achieving high power efficiency.

Keywords*: Biomedical Applications, Complementary SF-C, Low Voltage, LPF, Common Mode Bulk-feedback, Ultra low-power.*

Optimization of Mixed Sn and Pb Perovskite Solar Cell in Terms of Transport Layers and Absorber Layer Thickness Variation

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Abstract: The performance of the organic and inorganic halide perovskite solar cells (PSCs) has been improved rapidly in the last few years. In literature maximum PSCs are based on lead (Pb) based perovskite ($CH_3NH_3PbI_3$) and such PSCs have reflected record conversion efficiency of 25.2% in the year 2020. PSCs own some unique properties like excellent optical absorption, bandgap tunability and low fabrication cost. This makes hybrid PSCs most promising for photovoltaic (PV) industry by means of performance with power conversion efficiency (PCE). We in this work report the simulation study on a low bandgap (1.2eV) mixed Sn (50%) and Pb (50%) halide ($MAPb_{0.5}Sn_{0.5}I_3$) PSC structure. Initially a device with the combination of C_{60} (Buckminsterfullerene) and $IC_{60}BA$ (Indene-C_{60} Bisadduct) as electron transport layer (ETL) and PEDOT: PSS (poly(3,4-ethylenedioxythiophene) polystyrene sulfonate) as hole transport layer (HTL) respectively is calibrated. Thereafter, the analysis has been performed by using different set of HTLs like PEDOT: PSS, P3HT, Cu_2O and Spiro-OMeTAD in which highest PCE of 13.57% is achieved with C_{60} & $IC_{60}BA$ (ETL) and PEDOT: PSS (HTL). Followed by ETLs (mp-TiO_2 and CdS) variation which reflected the highest PCE (18.82%) with mp-TiO_2 (ETL) and PEDOT: PSS (HTL). The results are further summarized in terms of absorber layer thickness variation from 50 nm to 300 nm at the optimized ETL (mp-TiO_2) and HTL (PEDOT: PSS) material. The exercise carried out in this work showed optimized conversion efficiency of 19.21%. Work reported in these studies may open up the window for the development of low lead content perovskite based high efficiency PSCs.

Keywords*: Perovskite solar cells; Narrow bandgap halide (NBH); Electron transport layer (ETL); Hole transport layer (HTL); Absorber layer thickness; SCAPS-1D; Simulations.*

A Low Voltage NMOS current bleeding down conversion Mixer with source degeneration in 0.18µm CMOS technology

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Abstract: This article represent a little voltage, source degenerated CMOS down conversion mixer with NMOS current bleeding double balanced topology with resistive loads. Source degeneration with inductors proves out to be efficient in noise performance and linearity improvement. At, 0.9V of dc power supply and LO power of -2dB, this mixer has measured a conversion gain of 11dB, NF of 9.3 dB & IIP3 point of 6.11717dBm. This topology has been compared with a Modified current bleeding topology, conventional current bleeding topology and a simple double balanced topology; the results obtained suggest that the proposed topology has improved performance.

Keywords*: Radio Frequency; Intermediate Frequency; Local Oscillator; CMOS, Differential; Double balanced, Current Bleeding*

DFT Based approach to sense SF_6 decomposed gases (SO_2, SOF_2, SO_2F_2) using Ni doped WS_2 monolayer

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Abstract: *The potential of Sulfur hexafluoride, SF_6 decomposition gases (SO_2, SOF_2, SO_2F_2) adsorption on Ni-doped mono layer WS2 (SL-WS_2) has been studied using density function theory (DFT). The electro-chemical characteristics i.e. band structure analysis, density of states (DOS), adsorption distance as well as adsorption energy were discussed. Result suggest that the doping of Ni to mono layer WS_2 will drop in the band gap 27.5%. When SO_2, SOF_2, SO_2F_2 is adsorbed to Ni doped WS_2, the reduction of band gap can be noticed 25.4%, 44.88%, 67.18%, respectively. The adsorption energy study of SO_2, SOF_2, and SO_2F_2 also suggest that these gases chemisorbed on Ni doped WS_2. During the adsorption of SO_2F_2 on Ni of Ni doped WS_2, SO_2F_2 dissociated into two parts SO_2F and F. Simultaneously, the adsorption length between adsorbed and adsorbent also calculated.*

Keywords*: DFT; SF6; SL-WS2; adsorption energy (Ead); DOS*

Analytical Model for Tunnel Current in Semiconducting nano wire MOSFET

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Abstract—ITRS standard for effective oxide thickness (EOT) is projected to attain a value as low as 0.5nm by 2022, so as to get better control over the channel current and obviously to go for Ultra Large Scale Integration (ULSI). In doing so, major issue is the OFF state current or gate leakage current. People are using high-k dielectric to limit the OFF state current to a low value. But, planar configuration with Si technology has already gone down to its lowest limit. In search of better option, Si nanowire with gate around configuration can effectively suppress OFF state current with much larger ON current.
In order to incorporate Si nanowire MOSFET in integrated circuit a compact model for 1D transport needs to be developed considering the altered band structure and corresponding density of states and its dependence on the diameter of wire, shape of cross section, crystal orientation and interface states. In this article, we have tried to develop a model to determine gate leakage current considering 1D density of states of Si nanowire for the full regime of gate bias employing direct tunneling through dual oxides stack(SiO_2/HfO_2) used as gate dielectric. [001] crystal orientation having highest number of quantum channels and small effective mass is used for the analysis.

Keywords: *Density of states, MOSFET, quantum tunneling, WKB approximation.*

Analysis of electrical properties of unpolarized/polarized CNT-BNNT-CNT for varying lengths of BNNT

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Abstract: The study of the electronic and electrical properties of three different samples of CNT-BNNT-CNT was calculated using Density Functional Theory (DFT). The bandgap increases as the length of Boron Nitride Nanotube (BNNT) increases for both polarized and unpolarized samples which depicts the bandgap tunability of CNT-BNNT-CNT based heterostructure nanotube. The bandgap tunability finds application in nanophotonics, nanoelectronics, and Field Effect Transistor (FETs). From the Density of States (DOS) plot, the highest peak was observed in the conduction band for both the polarized and unpolarized CNT-BNNT-CNT samples. In the unpolarized sample, the highest peak was obtained for sample2 at energy 5eV with peak of $90000(eV)^{-1}$. For spin-polarized, the highest peak was obtained for sample3 at energy 2/-2eV with peak of $7000/-7000(eV)^{-1}$. Higher the availability of peak in DOS plots better is its application of spintronic memory devices. BNNT has its application in sensor membranes, memory devices and separation membrane for separating cations and anions. The research on BNNT is still in its early stages. Hence, it is highly promising for work study and future applications.

Keywords*: DFT, LCAO, DOS, BNNT, heterostructure nanotube*

First Principle Study of MoS_2 adsorbed Transition Metal for Sensing Urea and Methanol

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Abstract: Using the first principle calculation the sensing properties of the pristine MoS_2 and MoS_2 adsorbed with different transition metals (Co/Cu/Fe/Mn/V) were studied. The sensing materials used for our calculation are urea (CH_4N_2O) and methanol (CH_3OH). We analyzed whether the pristine or TM adsorbed MoS_2 were considered a better sensor. The bandstructure, density of states (DOS), and effective mass parameters were calculated using Density Functional Theory (DFT). The calculation was performed using Quantum ATK. We found out, among all the materials, MoS_2-Cu-CH_4N_2O has the highest DOS 500(eV)-1 at energy -2.2eV, implying it is a better sensing material for CH_4N_2O. They have the highest number of states available for occupancy. The energy bandgap was calculated for different transition metals. Among all the sensing material, we observed the maximum variation in bandgap for Fe adsorbed MoS_2 sensed with CH_3OH and CH_4N_2O and hence depicting it to be a superior sensing material. The effective mass of sample MoS_2 and Co adsorbed MoS_2 increases more when sensed with sensing material CH_3OH and CH_4N_2O.

***Keywords**: DFT, TMDs, adsorbed TM, MoS2, sensor*

First Principle Study of MoS_2 adsorbed Transition Metal for Sensing NH_3 and CH_4

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Abstract: Computational study of MoS_2 sensing material with adsorbed transition metal (Cu/Co/Fe/Mn/V) was studied. The first principle study was performed based on density function theory (DFT) to study properties such as bandstructure, the density of states (DOS), and effective mass using the Quantum ATK tool. We used Ammonia (NH_3) and Methane (CH_4) as sensing gas and found, among all the material MoS_2-Fe has the highest DOS 707 (eV)-1 at 1.4 eV when NH_3 sensing gas is added, which indicated it is better sensing material for NH_3 and has the highest number of states available for occupancy. From the calculation of bandgap, it is found that MoS_2 varies the most when NH_3 sensing gas is added from 1.6 eV to 0.36 eV making it a good material for sensors. We also calculated the effective mass of MoS_2 with adsorbed TM and found that the effective mass of the material increases more when NH_3 gas is added.

***Keywords**: TMDs, DFT, adsorbed TM, gas sensor, 2D material*