# Compact modeling of semiconductor devices in micro- and nanoelectronics

Daniel Tomaszewski

Łukasiewicz Research Network – Institute of Microelectronics and Microsystems, Warsaw, Poland

Abstract

A development of technological processes, a design of complete sequences of operations enabling manufacturing of micro- and nanoelectronicsemiconductor structures, a design of semiconductor devices and integrated circuits and their characterization are the basic stages of the so-called micro/nanoelectronictechnologies. Due to the complexity, these tasks are carried out using computer techniques, including tools for technology computer-aided design (TCAD) and for Electronic Design Automation (EDA). Sophisticated computational models of technological processes and advanced models of semiconductor structures are used in the TCAD tools, including charge carrierstatistics and transport in semiconductors, heat transport, stress propagation etc. In the EDA tools the compact models of semiconductor devices are implemented. The models from different categories support the aforementioned technology development tasks not only as computational tools but also as a platform to facilitate understanding of complex technological processes and operation of semiconductor devices.

The semiconductor device models take into account numerous physical phenomena, which are coupled with each other, in particular in the state-of-the art scaled devices. However, these phenomena are very often identified separately based on considerations of large size devices or devices operated at specific conditions in which mechanisms of interest are highlighted.It should be noted that the integration of the fragmentary models is probably the most difficult stage in the construction of the complete models because it requires the reconciliation of numerous and sometimes mutually inconsistent assumptions underlying the component models.

For many years the bulk and silicon-on-insulator (SOI)complementary metal-oxide-semiconductor (CMOS) and bipolar integrated circuit technologieshave been main targets of the semiconductor process and device modeling. However, thetechnologies for alternative devices(e.g. tunnel FETs, ferroelectric FETs, FinFETs nanowire NWFETs), bipolar devices (heterojunction bipolar transistors – HBTs), high power electronics (e.g. AlGaN/GaN, SiC), thin film organic and oxide transistors, to name a few, have come into play. In this talk I will present selected aspects of the semiconductor devicecompact modeling and its application for micro/nanoelectronic technologycharacterization, and for integrated circuitdesign.